

# GIGABYTE GA-8IP900

# Schematics

Revision 1.01

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3,4 CHANNEL B
13	DDR TERMINATION
14	AGP 8X SLOT
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	DUAL FWH
19	CY28405 CLOCK GENERATOR
20	PCI SLOT1/SLOT2
21	PCI SLOT3/SLOT4/RESET BUFFER
22	PCI SLOT5/SLOT6

SHEET	TITLE
23	AC '97 CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712/IR_CIR/SCR/S_IRQ
26	COMA/VGA_COMB/LPT
27	IDE1/IDE2/FDD
28	FAN/HW MONITOR
29	KB_MS/GAME/FUSEVCC
30	FRONT PANEL
31	R_USB/F_USB1/F_USB2
32	DDR/VDDQ/5VDUAL/VCCVID POWER
33	VCORE POWER
34	ATX/ATX_12V/FAN1655M
35	KINNERETH-R LAN(CSA-1)
36	KINNERETH-R LAN(CSA-2)
37	KINNERETH-R LAN(CSA-3)
38	TI TSB43AB23(1394)
39	SIL3112/TQFP(S-ATA)
40	PCI ROUNTIONG
41	GPIO PIN LIST

PROCESS: C	COMPONENT SIDE (0.5 oz. Copper)
_____	VCC SIDE (1 oz. Copper)
_____	GND SIDE (1 oz. Copper)
_____	SOLDER SIDE (0.5 oz. Copper)
_____	

**GIGABYTE CORP.**

Title		COVER SHEET	
Size	Document Number	GA-8IP900	Rev
Custom			1.01
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Model Name: GA-8IP900

Version : 1.01

### Circuit or PCB layout history

### Component history

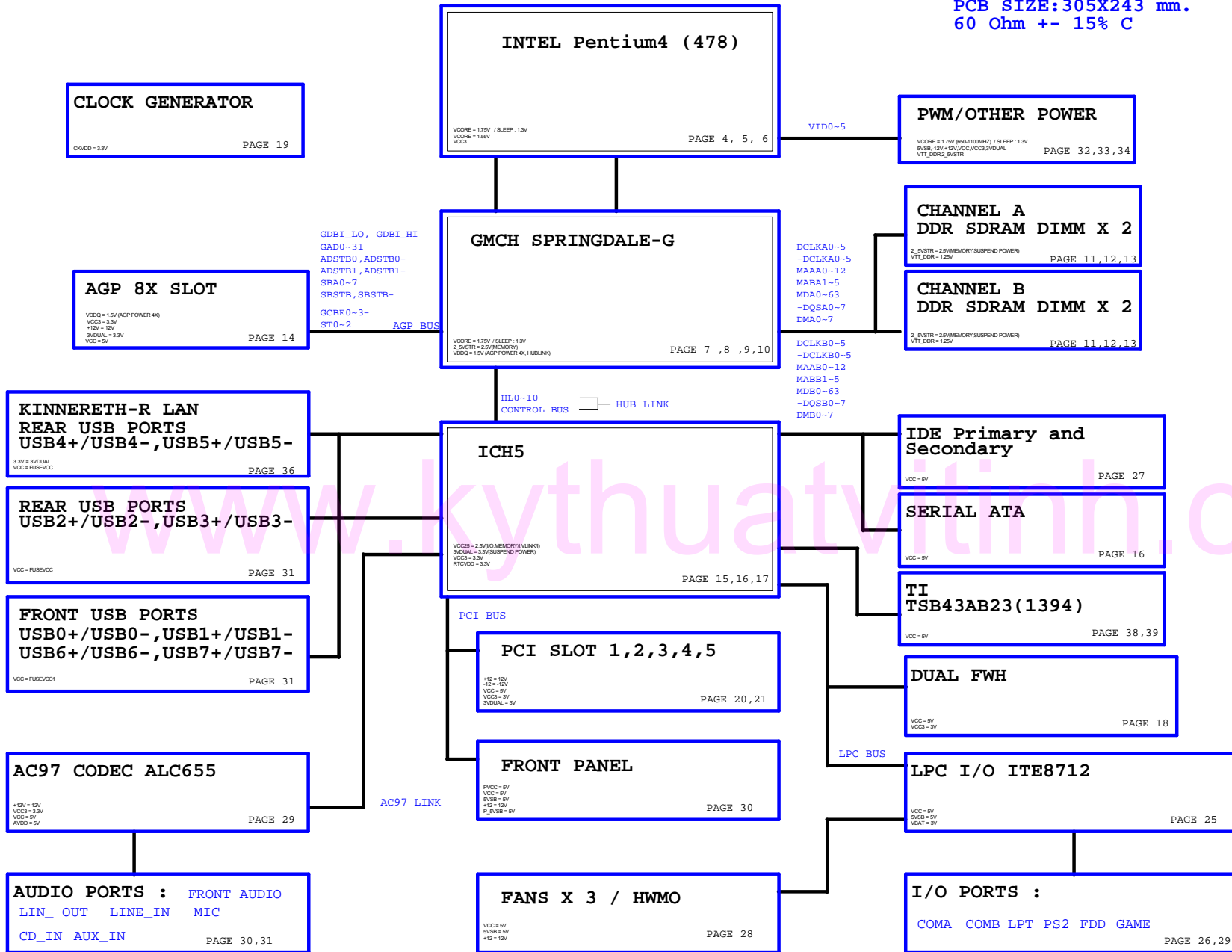
Date	Change Item	Reason
1/10 (0.1A)	Add B59,BC61,BC64,BC65,BC70,BC74,BC75,BC81,BC84,BC91,BC513,BC549,BC550 : 0.1U/6 SMD CAP.	Modify power ripple.
	Add C362,C380,C381 :4.7U/8 SMD CAP.	
	Add CN2,CN7,CN8,CN10,CN11,CN13,CN14,CN19,CN24,CN27 :0.1U/8P4C SMD CAP.	
	Add EC4,EC69,EC81,EC82,EC120 :100U/10V/57 DIP CAP.	
	Add R814 :2.2/6 SMD resistor.	
	Add R671 :8.2K/6 SMD resistor.	Modify clock GEN. strapping.
1/29 (0.2)	X2 14.318 change to 16pf.	Modify 14.318Mhz.
	C255,C256 change to 20pf.	Modify 14.318Mhz.
	R28,R31 change to 1K/6.	FS A/FS_B level.
	R583 change to 2.2K/6.	Power LED.
	R13 change to 2.2K/6.	VCCVID POWER GOOD.
	Add CX1 24.576MHZ.	CODEC 650 clock.
	Add CBC53 0.1U.	Front audio MIC.
	R822 470K/6 remove.	Modify CPU Vcore.
	Add R830 20K/6.	
	R1103 chage to 2.26K/6/1 R1104 chage to 1K/6/1	Modify DDR voltage.
	Delete BC322,BC301 compoment.	BOM error.
(0.3)	ADD TI1394 AND SII (S-ATA)	
(1.0A)	BATTERY SOCKET 改高 PCB 0.3 >1.0 凡COPY 此PROJRCT 請將3VDUAL1 改成3VDUAL 切記	
(1.01)	修改文字面 (Dual Bios移除 , DDR400 -->DDR )	

Date	Change Item	Reason
0.2	Support WILLAMETTE CPU Add CEC4 for CODEC power. VGA 水波紋 S-IRQ,NB_FAN 改防呆 USB,1394 change to housing. Vcore transient power. N.B reference power.	
1.0 A	由81PE1000PRO REV0.3 修改	
1.0 B	PCB 1.0 CHANGE TO 1.01 C211 100P/4 CHANGE TO 100P/4 CBC53 0.1U/6 CHANGE TO 1U/6 C250,C358,C230 ADD 10P/4 BC395,BC398 0.1U/6耐壓12V BC331 1U/6 BC401,BC336 1U/6 Q100 MMBT2222 CHANGE TO BAT54A R752 8.2K/6 REMOVE REMOVE 12LB6-ICPU1IT-00(STICK FOR INTEL P4CPUHT	FOR F_MIC FOR EMI FOR EMI FOR EMI FOR DUAL BIOS 切換 FOR DUAL BIOS 切換
1.0C	REMOVE Q201 REMOVE EC124,EC125 1000U , BC572 REMOVE R1176 100/6,R1175 392/6/1,R1177 1K/6/1 F USB1_2 BOX HEADER --> PIN HEADER	REMOVE VDD18 POWER (SIL3112 POWER) REMOVE VDD18 POWER (SIL3112 POWER) REMOVE VDD18 POWER (SIL3112 POWER)
1.0D		

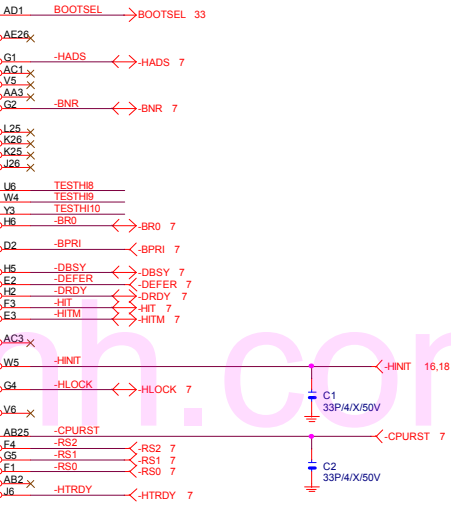
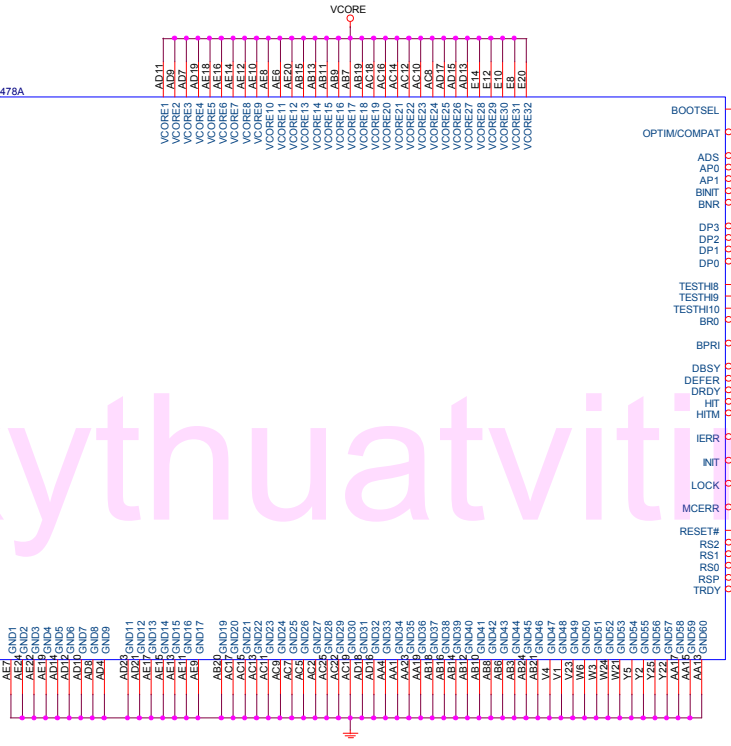
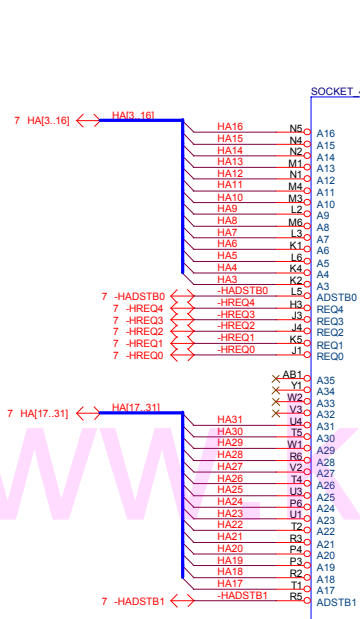
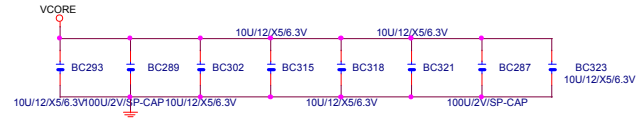
<b>GIGABYTE CORP.</b>			
Title <b>BOM &amp; PCB MODIFY HISTORY</b>			
Size Custom	Document Number <b>GA-8IP900</b>	Rev <b>1.01</b>	
Date	1 Sheet 2 of 41		

# BLOCK DIAGRAM

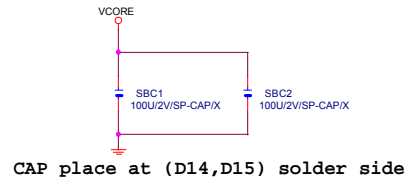
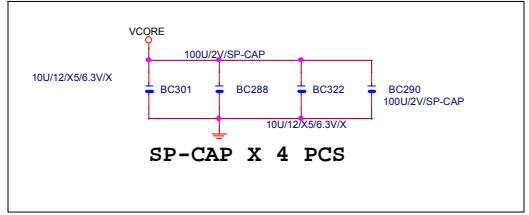
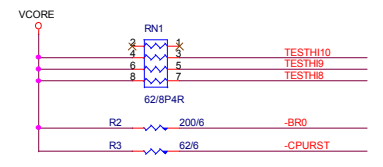
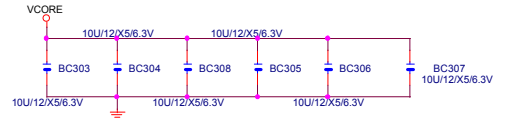
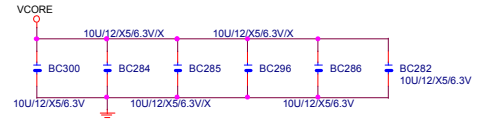
PCB SIZE: 305X243 mm.  
60 Ohm +/- 15% C



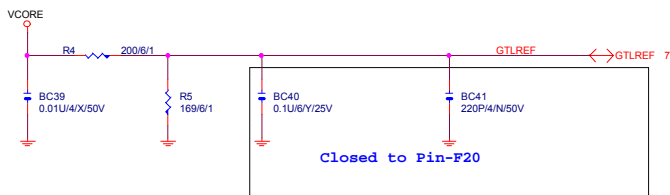
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BOM & PCB MODIFY HISTORY			
File	Document Number	GA-SIP900	Rev
Size	1.0		
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Date			



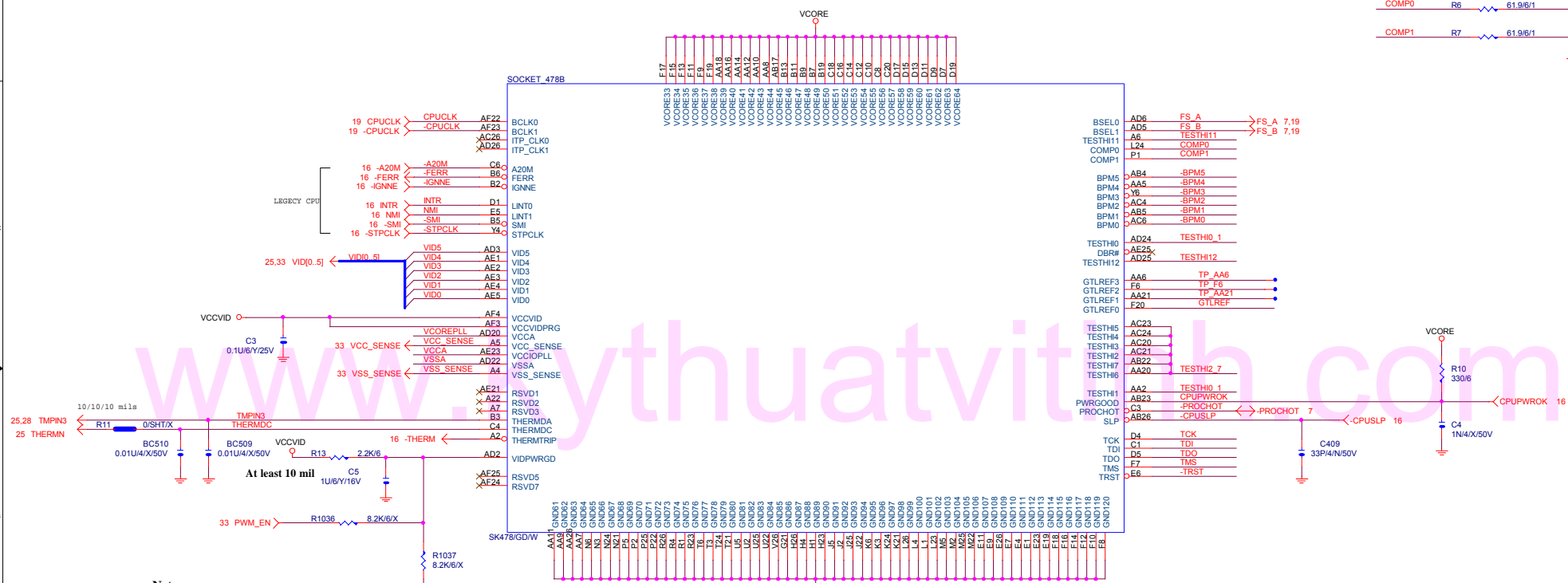
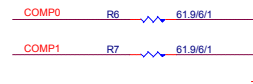
**CPU SOCKET**



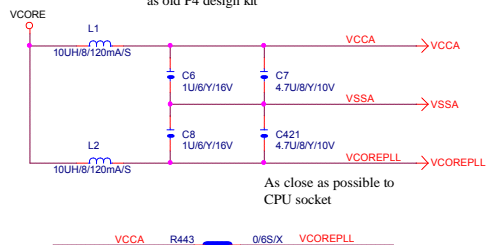
Title			P4 478A		
Size	Document Number	GA-8IP900			Rev
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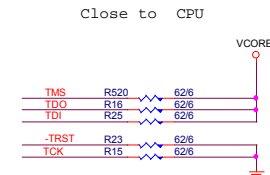
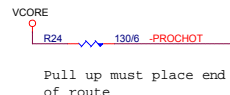
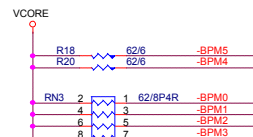
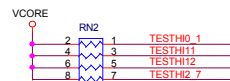
Place outside of CPU socket



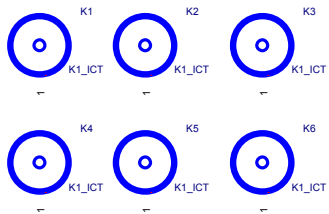
Note:  
VCCA & VCCOREPLL define doesn't same as old P4 design kit



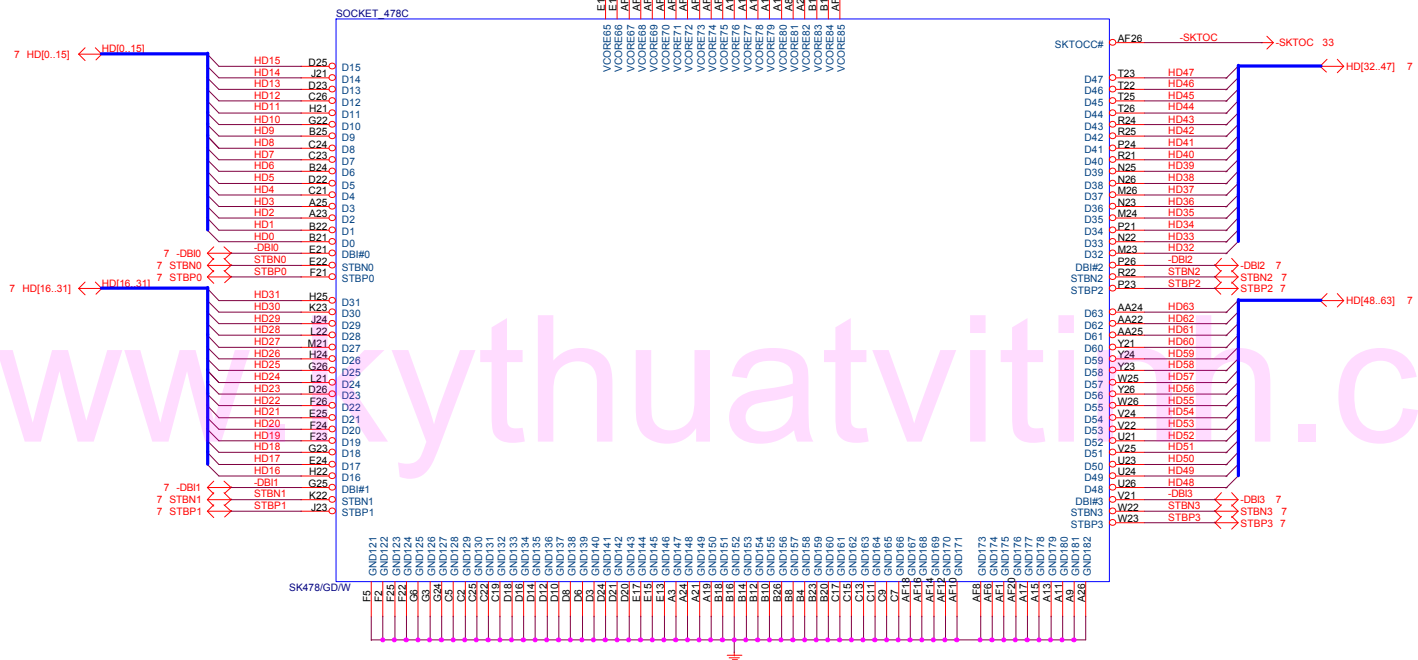
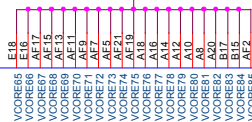
Trace width doesn't less than 12 Mil



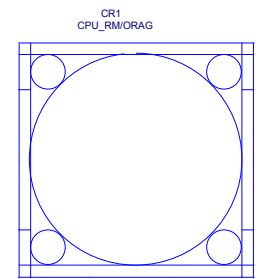
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Size	Document Number			Rev	1.01
Custom	GA-8IP900				
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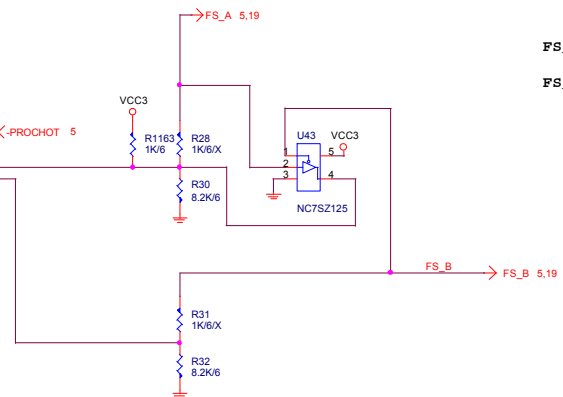
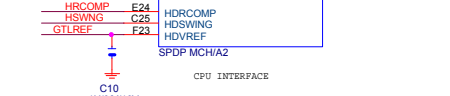
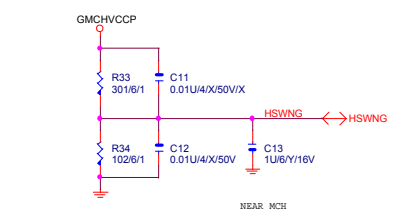
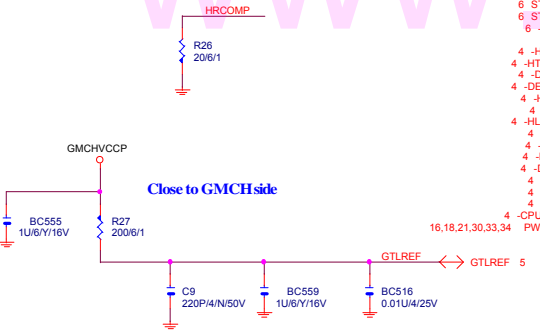
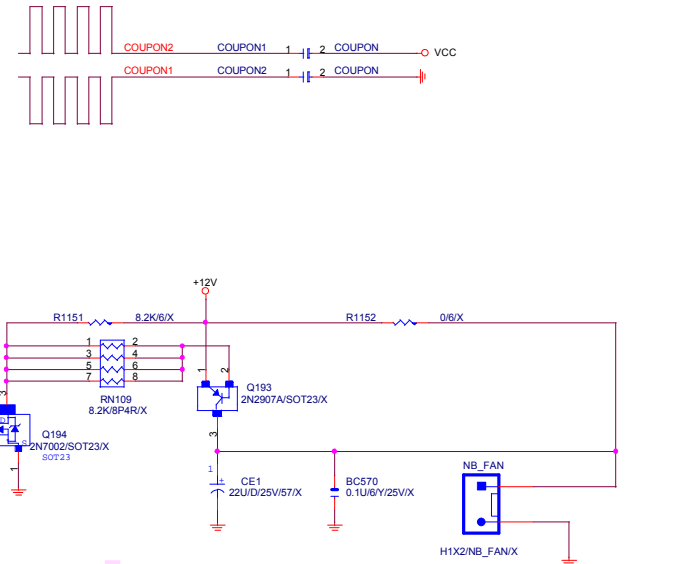
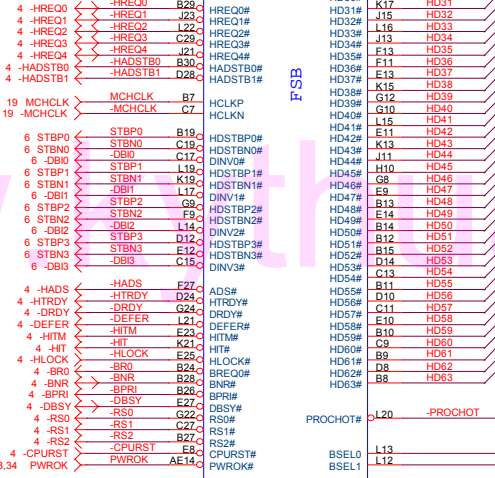
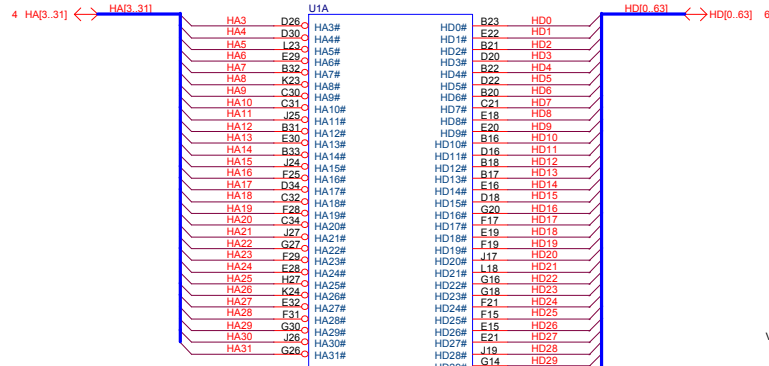
VCORE



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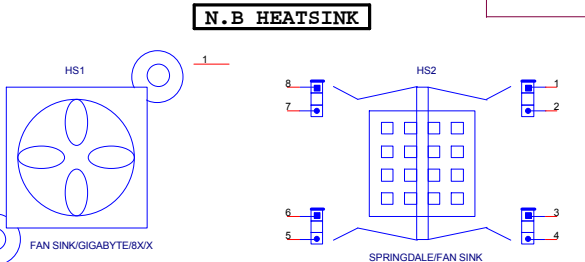


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Size	Document Number				Rev
Custom	GA-8IP900				1.01
Date	Sheet 6 of 41				

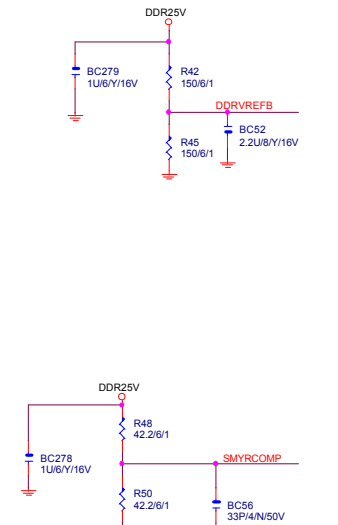
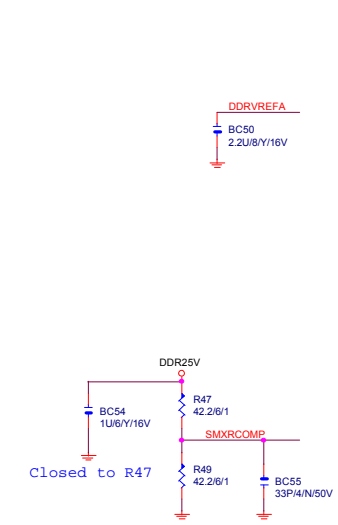
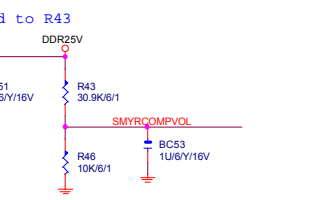
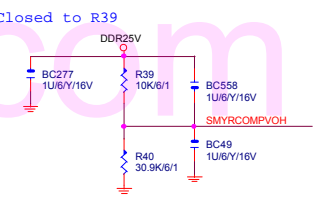
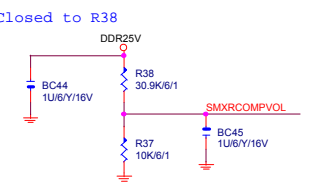
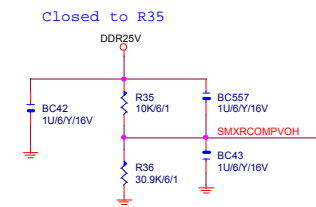
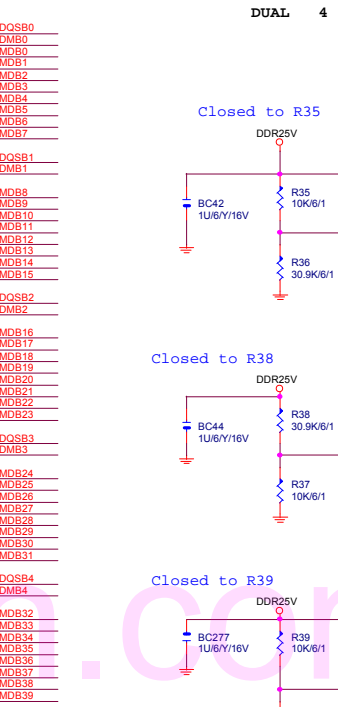
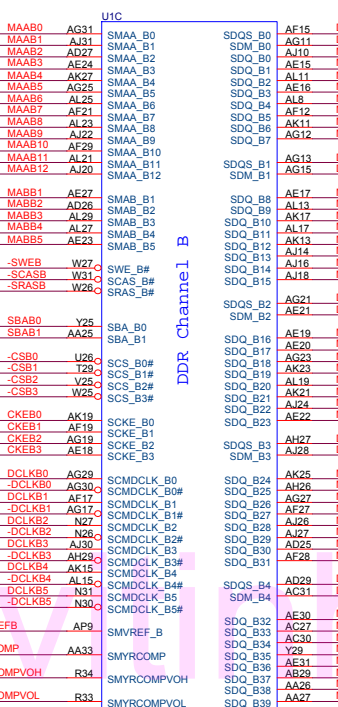
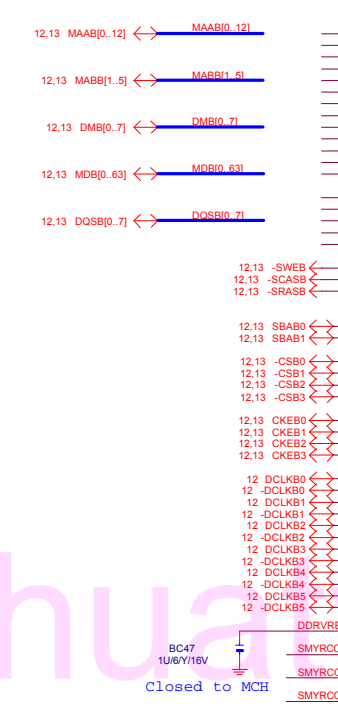
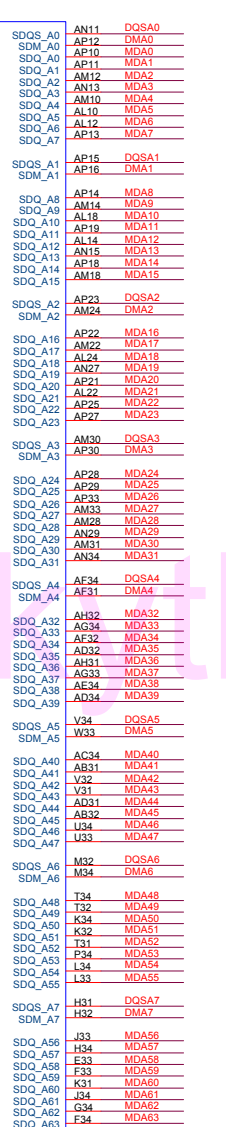
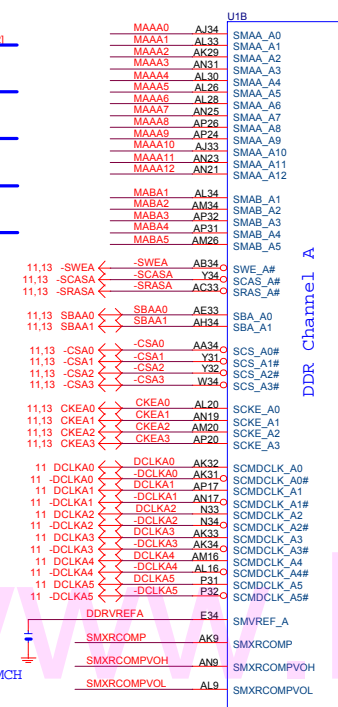
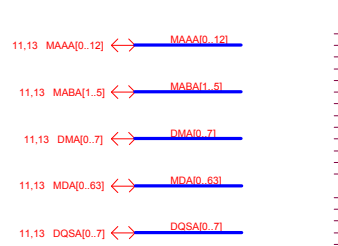


	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X1.33	X1.6
X2.66	X2.5	X1.6	X2

FOR SPD P (533MHZ)  
REMOVE R28, R31  
ADD R1163, U39,



DDR 400 1-2-3-4 CPC DISABLE  
 DDR 333 SIGNAL 1 CPC ENABLE  
 2 CPC DISABLE  
 DUAL 2 CPC ENABLE  
 DUAL 4 CPC DISABLE





14 GAD[0..31] <-> GAD[0..31]  
 14 SBA[0..7] <-> SBA[0..7]  
 15 HL[0..10] <-> HL[0..10]

14 -GCBE0 <-> -GCBE0 Y7  
 14 -GCBE1 <-> -GCBE1 W5  
 14 -GCBE2 <-> -GCBE2 AA3  
 14 -GCBE3 <-> -GCBE3 U2

14 -GFRAME <-> -GFRAME U6  
 19 GMCH3V66 <-> GMCH3V66 U14  
 14 -GDEVSEL <-> -GDEVSEL AB4  
 14 -GIRDY <-> -GIRDY V11  
 14 -GTRDY <-> -GTRDY AB5  
 14 -GSTOP <-> -GSTOP W11  
 14 GPAR <-> GPAR AB2  
 14 -GREQ <-> -GREQ N6  
 14 -GGNT <-> -GGNT M7

14 GSWING <-> GRCOMP AC2  
 14 MCH\_AGPREF <-> MCH\_AGPREF AD2  
 14 -RBF <-> -RBF R10  
 14 -WBF <-> -WBF R9  
 14 -PIPE <-> -PIPE M4  
 14 GDBI\_LO <-> GDBI\_LO M5

14 ST0 <-> ST0 N3  
 14 ST1 <-> ST1 N5  
 14 ST2 <-> ST2 N2

HL0 <-> AF5 H0  
 HL1 <-> AG3 H1  
 HL2 <-> AK2 H2  
 HL3 <-> AG5 H3  
 HL4 <-> AK5 H4  
 HL5 <-> AL3 H5  
 HL6 <-> AL2 H6  
 HL7 <-> AL4 H7  
 HL8 <-> AJ2 H8  
 HL9 <-> AJ2 H9  
 HL10 <-> AJ3 H10

15 HLSTBF <-> HLSTBF AH5  
 15 HLSTBS <-> HLSTBS AH4

HLRCOMP\_MCH <-> HLRCOMP AD4  
 HL\_SWING\_MCH <-> HL\_SWING AE3  
 HL\_VREF\_MCH <-> HL\_VREF AE2

U1D  
 GADSTBF0 AC6 ADSTB0 <-> ADSTB0 14  
 GADSTBS0 AC5 ADSTB0 <-> ADSTB0 14

GAD0 AE6 GAD0  
 GAD1 AC11 GAD1  
 GAD2 AD5 GAD2  
 GAD3 AE5 GAD3  
 GAD4 AA10 GAD4  
 GAD5 AC9 GAD5  
 GAD6 AB11 GAD6  
 GAD7 AB7 GAD7  
 GAD8 AA9 GAD8  
 GAD9 AA6 GAD9  
 GAD10 AA5 GAD10  
 GAD11 W10 GAD11  
 GAD12 AA11 GAD12  
 GAD13 W6 GAD13  
 GAD14 W9 GAD14  
 GAD15 V7 GAD15

GAD16 AA2 GAD16  
 GAD17 Y4 GAD17  
 GAD18 Y2 GAD18  
 GAD19 W2 GAD19  
 GAD20 Y5 GAD20  
 GAD21 V2 GAD21  
 GAD22 W3 GAD22  
 GAD23 U3 GAD23  
 GAD24 T2 GAD24  
 GAD25 T4 GAD25  
 GAD26 T5 GAD26  
 GAD27 R2 GAD27  
 GAD28 P2 GAD28  
 GAD29 P5 GAD29  
 GAD30 P4 GAD30  
 GAD31 M2 GAD31

GSBSTF TI1 SBSTB <-> SBSTB 14  
 GSBSBTS TI1 SBSTB <-> SBSTB 14

GSBA0# R6 SBA0  
 GSBA1# P7 SBA1  
 GSBA2# R3 SBA2  
 GSBA3# R5 SBA3  
 GSBA4# U9 SBA4  
 GSBA5# U5 SBA5  
 GSBA6# U6 SBA6  
 GSBA7# T7 SBA7

H3 DDCA\_DATA  
 F2 DDCA\_CLK  
 E4 RED  
 H6 RED#  
 H6 GREEN  
 G5 GREEN#  
 H7 BLUE  
 G6 BLUE#  
 G3 HSYNC  
 F2 VSYNC

REFSET D2 REFSET R67 <-> REFSET  
 RESERVED\_1 NC\_1 A3  
 RESERVED\_2 NC\_2 A33  
 RESERVED\_3 NC\_3 AF13  
 RESERVED\_4 NC\_4 AF23  
 RESERVED\_5 NC\_5 AJ12  
 RESERVED\_6 NC\_6 AN1  
 RESERVED\_7 NC\_7 AN1  
 RESERVED\_8 NC\_8 AP2  
 RESERVED\_9 NC\_9 AR3  
 RESERVED\_10 NC\_10 AR33  
 RESERVED\_11 NC\_11 AR35  
 RESERVED\_12 NC\_12 B2  
 RESERVED\_13 NC\_13 B25  
 RESERVED\_14 NC\_14 B34  
 RESERVED\_15 NC\_15 C1  
 RESERVED\_16 NC\_16 C23  
 RESERVED\_17 NC\_17 C35  
 RESERVED\_18 NC\_18 E26  
 RESERVED\_19 NC\_19 M31  
 RESERVED\_20 NC\_20 R25

GRCOMP AC2 GRCOMP  
 GSWING AC3 GSWING  
 MCH\_AGPREF AD2 GRCOMP  
 MCH\_AGPREF AD2 GRCOMP

GRBF R10 GRBF  
 GWBF R9 GWBF  
 DBI\_HI M4 DBI\_HI  
 DBI\_LO M5 DBI\_LO

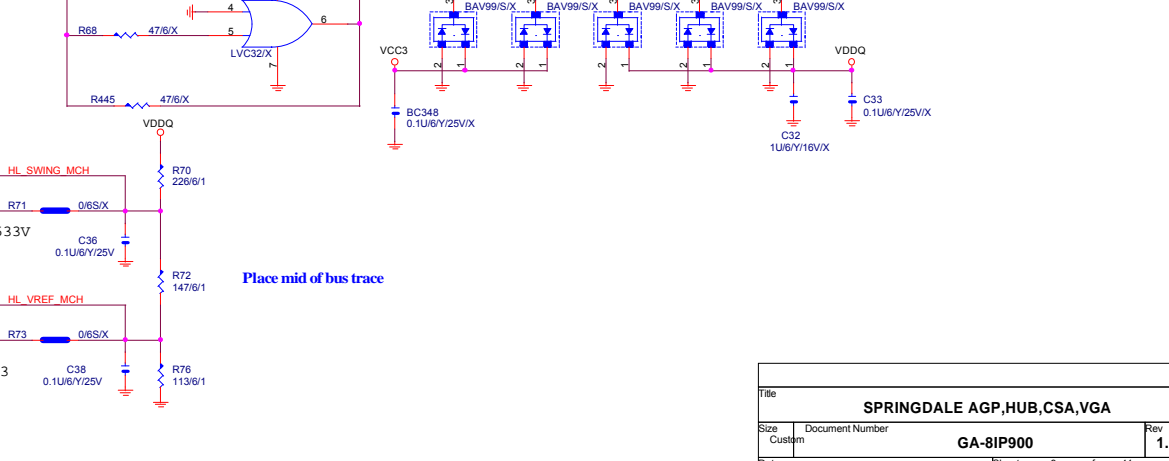
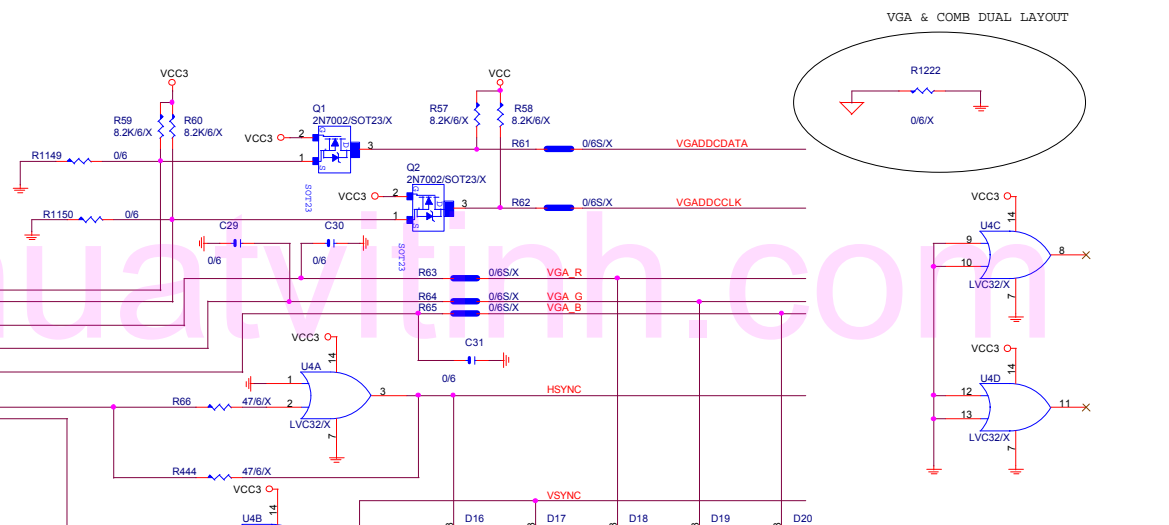
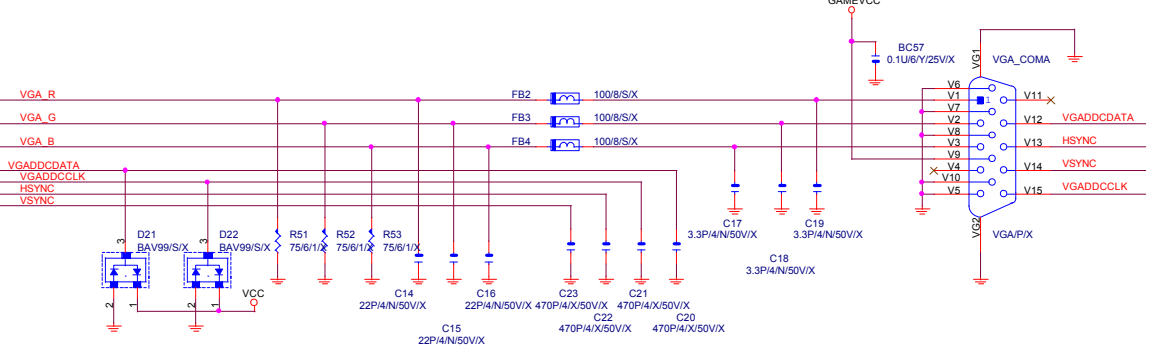
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 HL\_SWING\_MCH AE3 HL\_SWING  
 HL\_VREF\_MCH AE2 HL\_VREF

CLRCOMP AG2 CLRCOMP  
 CLSWING\_SPG AF2 CLSWING\_SPG  
 CLVREF\_SPG AF4 CLVREF\_SPG

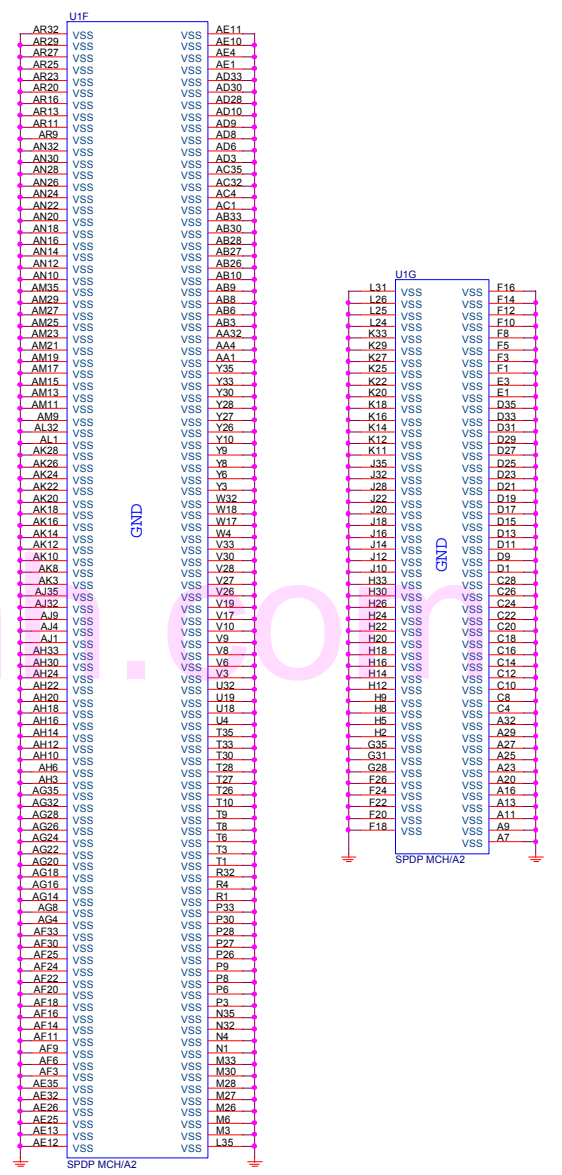
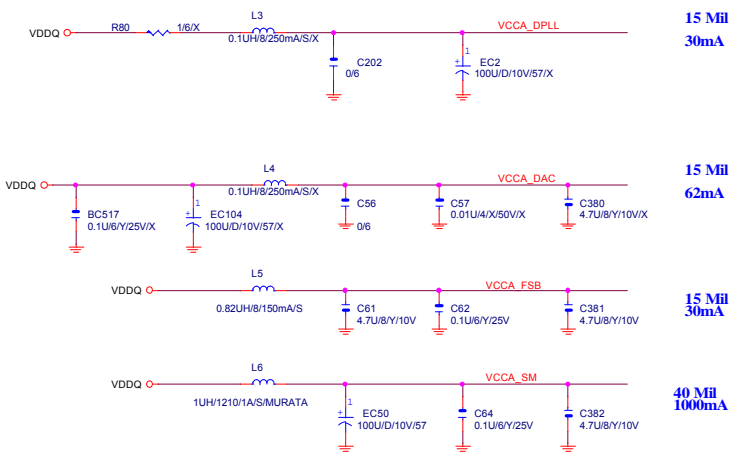
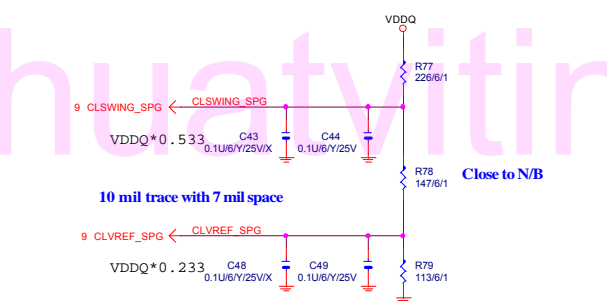
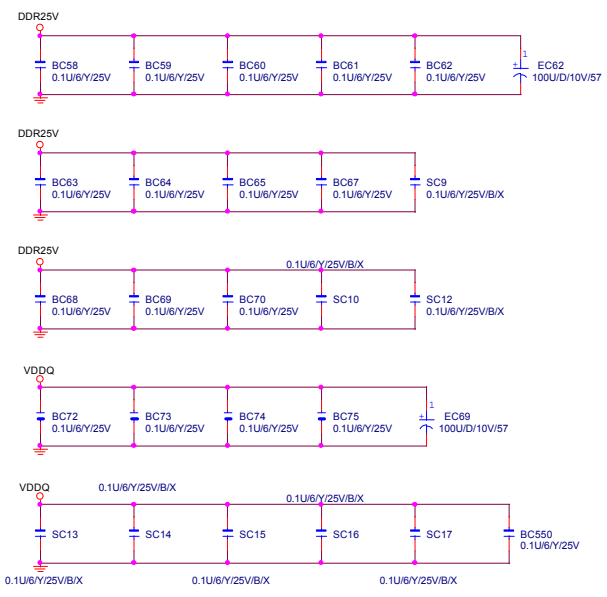
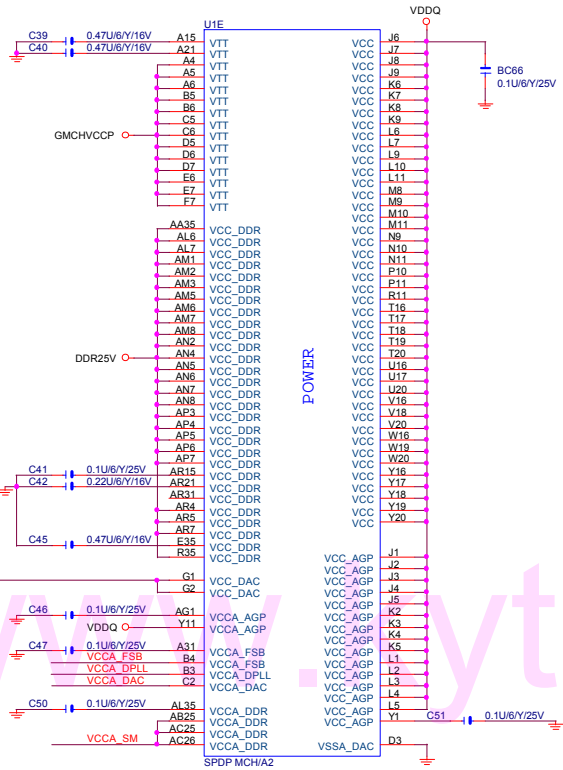
DOTCLK G4 DOTCLK  
 TP\_GMCH AP8 TP\_GMCH AP8  
 TP\_GMCH AG9 TP\_GMCH AG9

RESERVED\_1 NC\_1 A3  
 RESERVED\_2 NC\_2 A33  
 RESERVED\_3 NC\_3 AF13  
 RESERVED\_4 NC\_4 AF23  
 RESERVED\_5 NC\_5 AJ12  
 RESERVED\_6 NC\_6 AN1  
 RESERVED\_7 NC\_7 AN1  
 RESERVED\_8 NC\_8 AP2  
 RESERVED\_9 NC\_9 AR3  
 RESERVED\_10 NC\_10 AR33  
 RESERVED\_11 NC\_11 AR35  
 RESERVED\_12 NC\_12 B2  
 RESERVED\_13 NC\_13 B25  
 RESERVED\_14 NC\_14 B34  
 RESERVED\_15 NC\_15 C1  
 RESERVED\_16 NC\_16 C23  
 RESERVED\_17 NC\_17 C35  
 RESERVED\_18 NC\_18 E26  
 RESERVED\_19 NC\_19 M31  
 RESERVED\_20 NC\_20 R25

SPDP MCH/A2



Title		
SPRINGDALE AGP,HUB,CSA,VGA		
Size	Document Number	Rev
Custom	GA-8IP900	1.01
Date	Sheet	9 of 41



9 CLSWING\_SPG ← CLSWING\_SPG

VDDQ \* 0.533

10 mil trace with 7 mil space

9 CLVREF\_SPG ← CLVREF\_SPG

VDDQ \* 0.233

Close to N/B

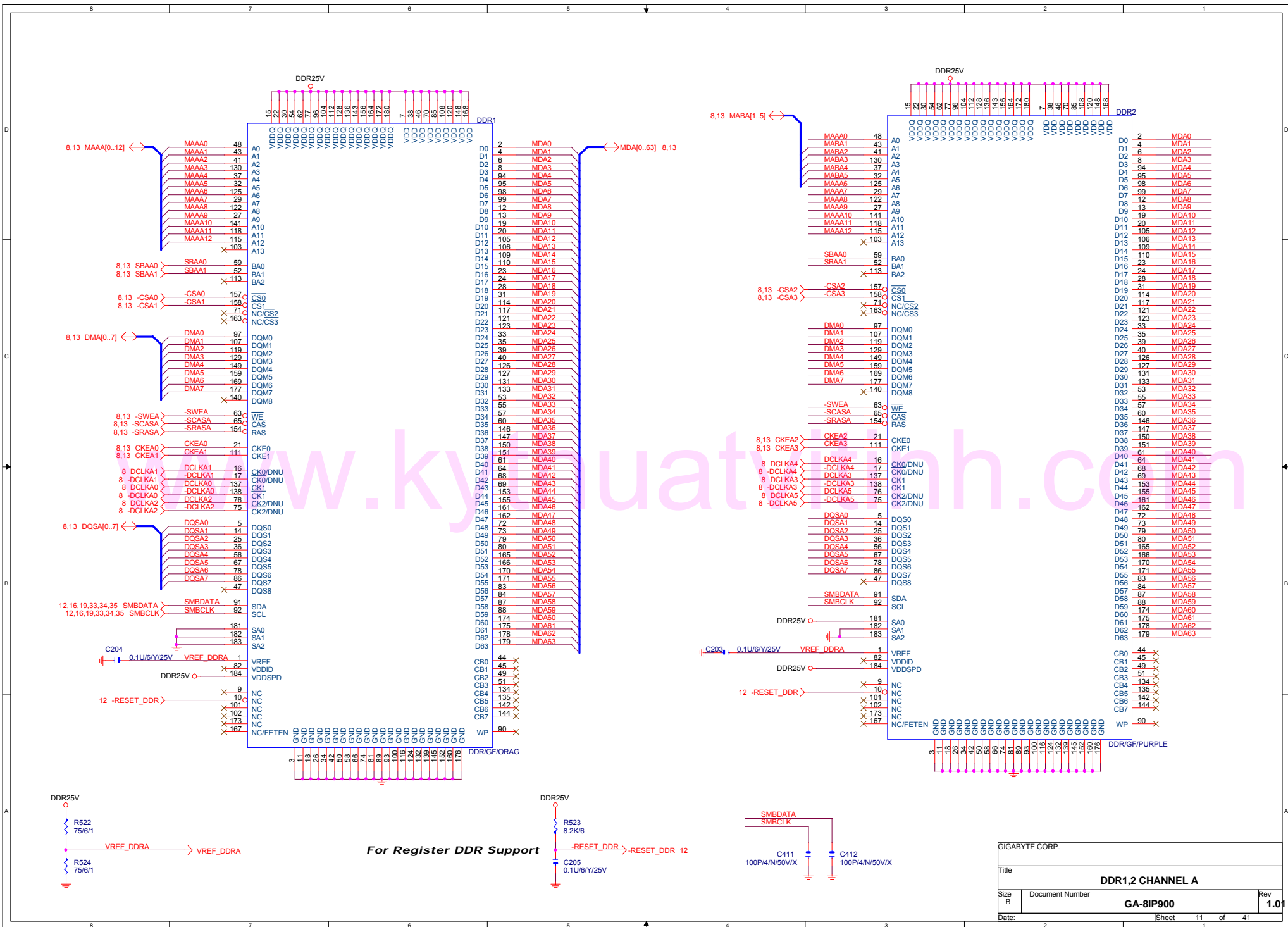
15 Mil 30mA

15 Mil 62mA

15 Mil 30mA

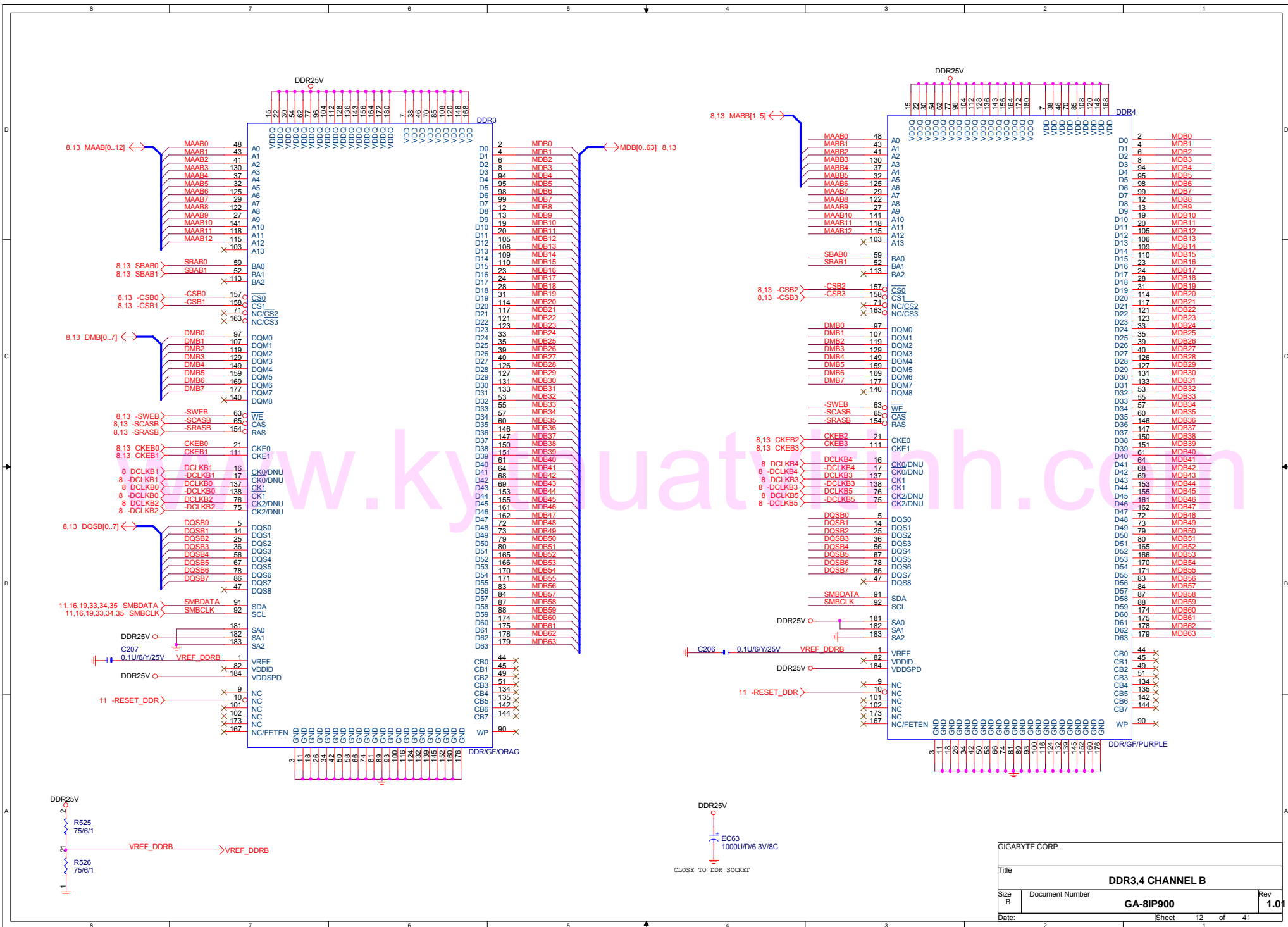
40 Mil 1000mA

Title			
SPRINGDALE PWR			
Size	Document Number	Rev	
Custom	GA-8IP900	1.01	
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For Register DDR Support

GIGABYTE CORP.		
Title		
<b>DDR1,2 CHANNEL A</b>		
Size	Document Number	Rev
B	GA-8IP900	1.01
Date:	Sheet 11 of 41	



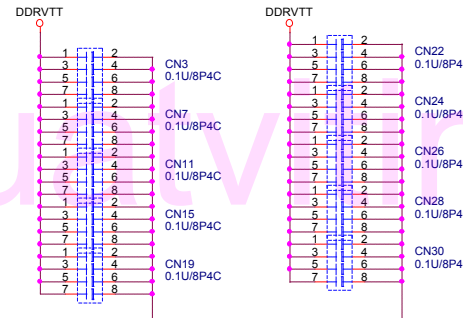
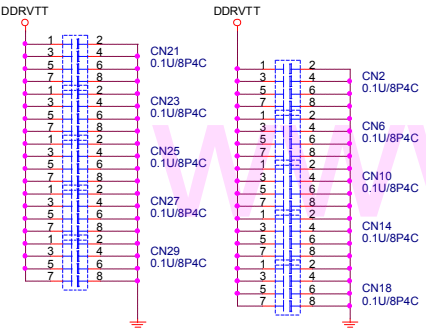
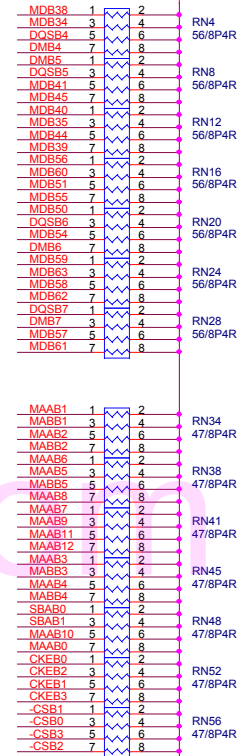
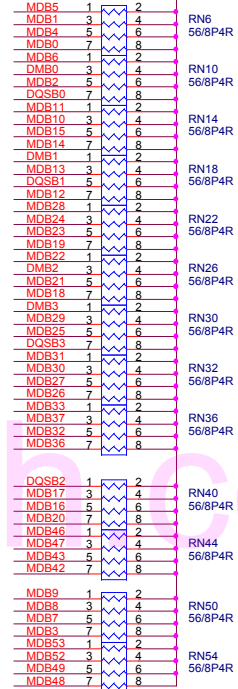
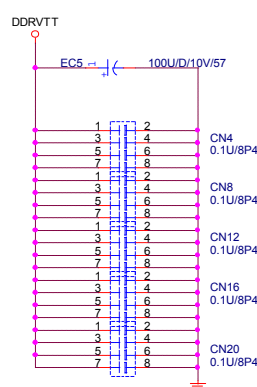
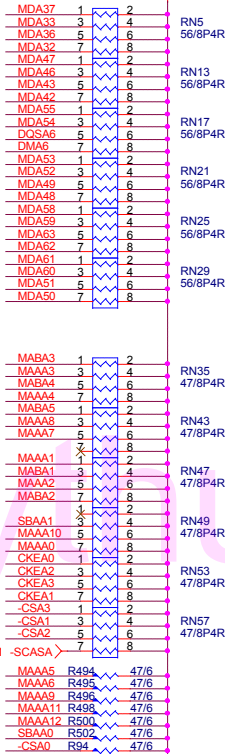
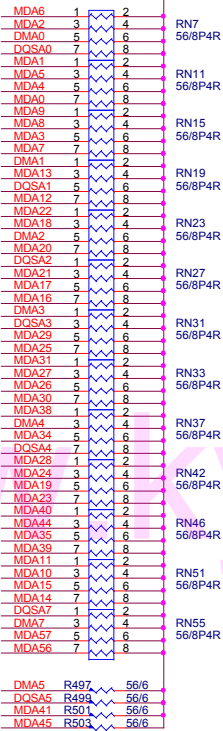
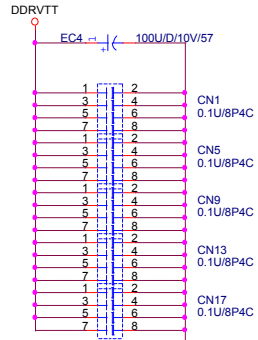
GIGABYTE CORP.		
Title		
<b>DDR3,4 CHANNEL B</b>		
Size	Document Number	Rev
B	<b>GA-8IP900</b>	<b>1.01</b>
Date:	Sheet 12 of 41	

DDRVTT Decouple

DDR TERMINATION CHANNEL A

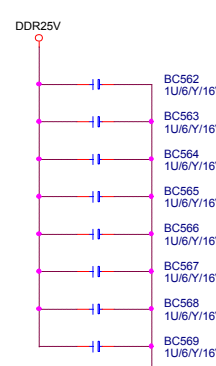
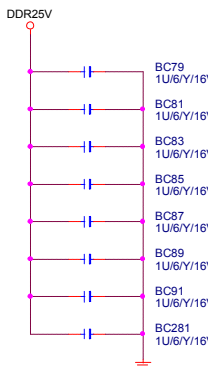
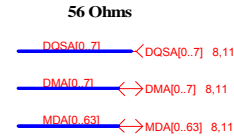
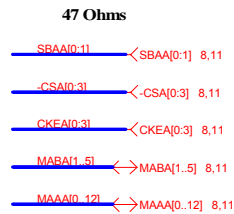
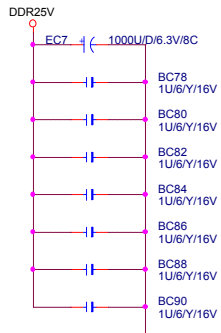
DDRVTT Decouple

CHANNEL B

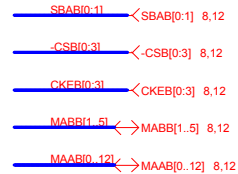


DDR25V Decouple

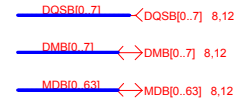
DDR25V Decouple



47 Ohms



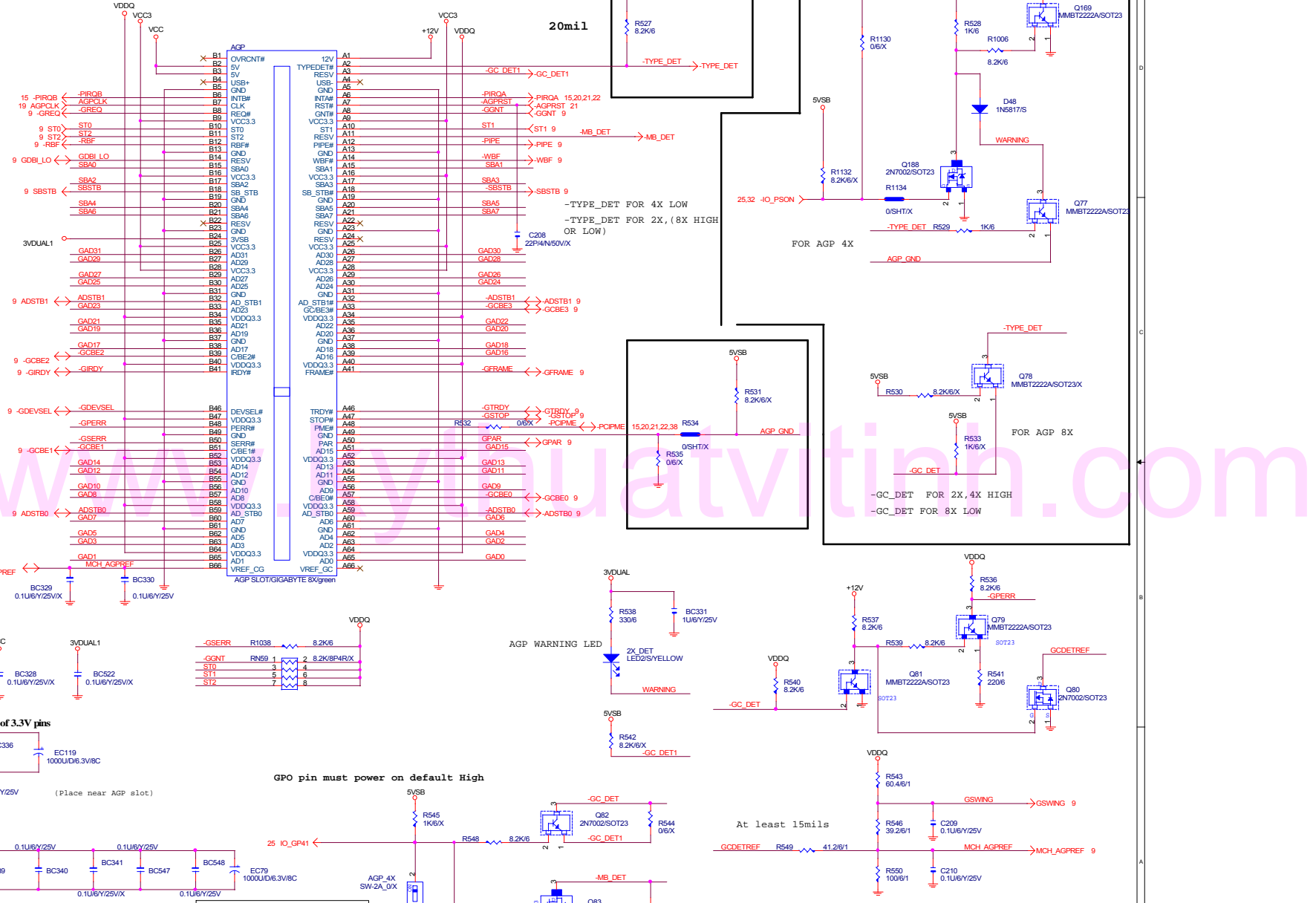
56 Ohms



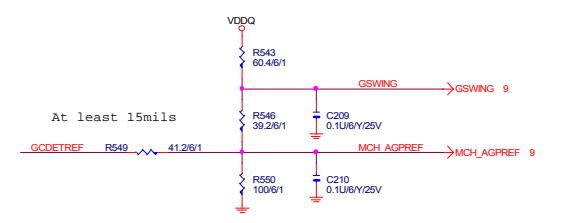
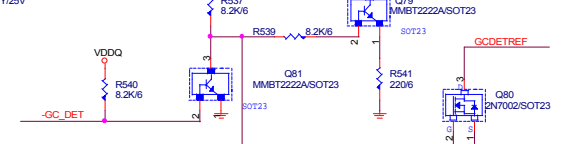
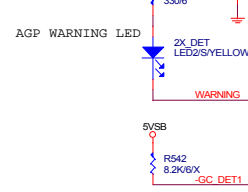
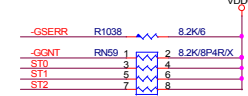
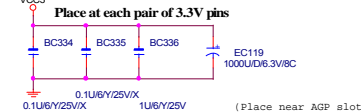
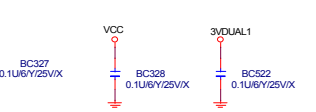
9 SBA0:7I ← SBA0:7I  
 9 GAD0:31K ← GAD0:31K

### AGP 4X/8X

20mil



www.atvitinh.com



GPO pin must power on default High

AGP_4X:	
ON	AGP 4X
OFF	AGP 8X

Place 1 at each pair of VDDQ pins  
 Place an additional for spread from A14- A33

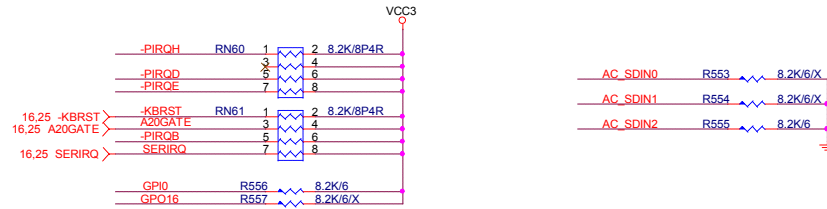
**GIGABYTE CORP.**

Title: AGP SLOT  
 GA-8IP900

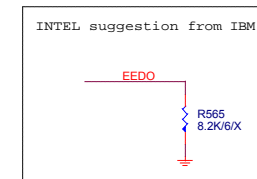
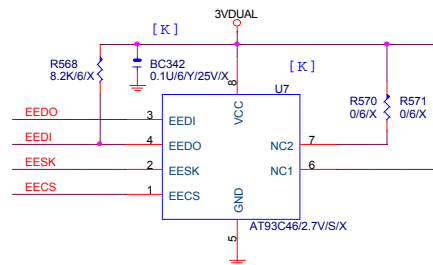
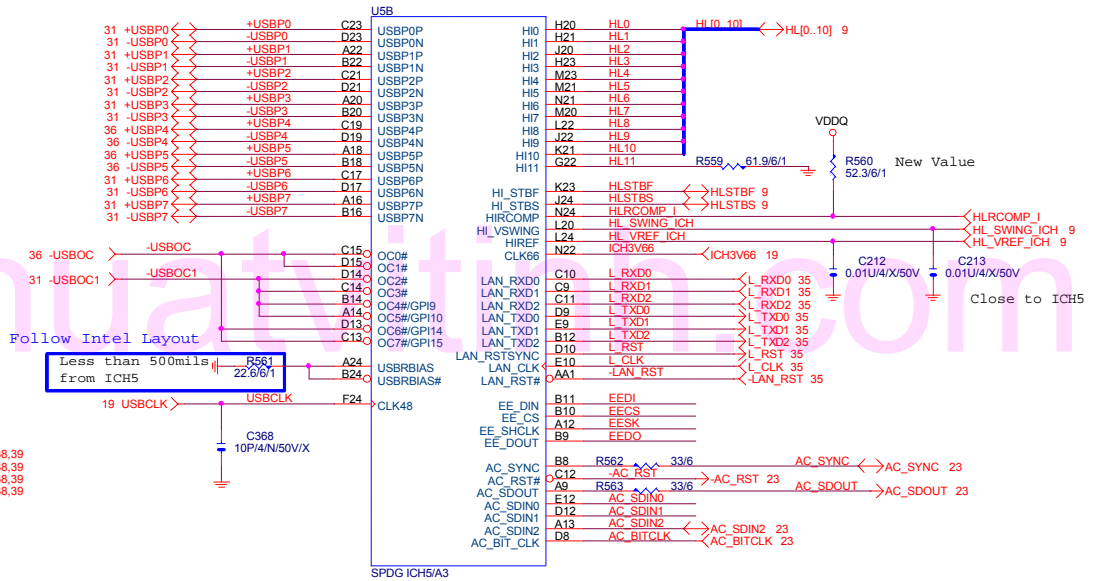
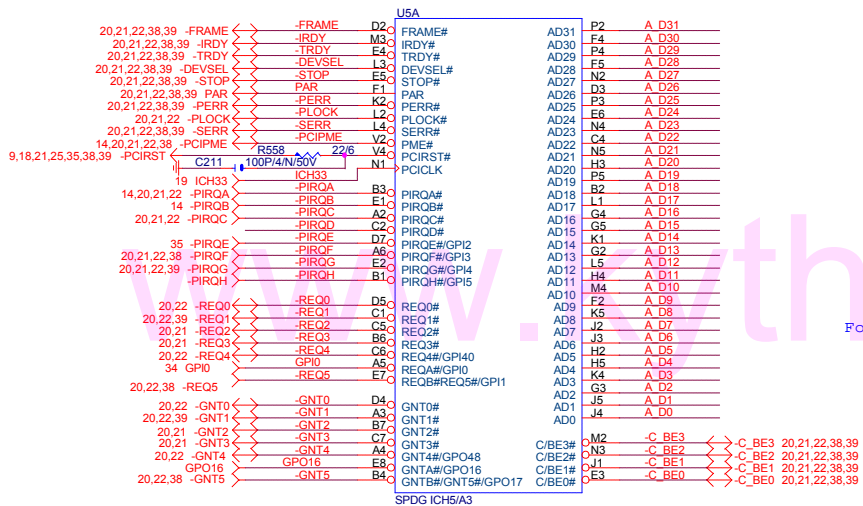
Size: Custom	Document Number:	Rev: 1.01
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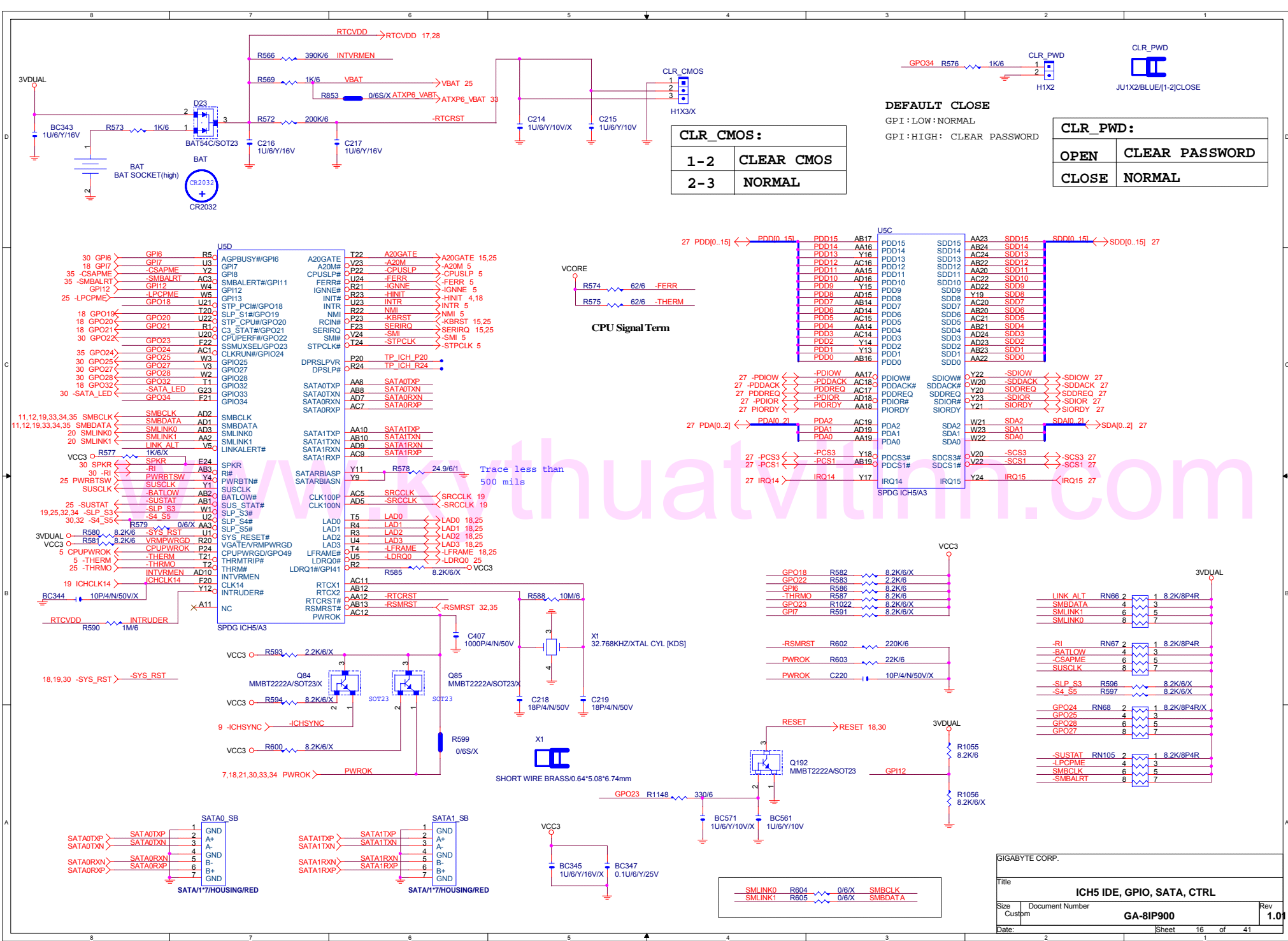
Date: Wednesday, April 16, 2003 Sheet 14 of 41





A\_D0[.31] <-> A\_D0[.31] 20.21,22,38,39



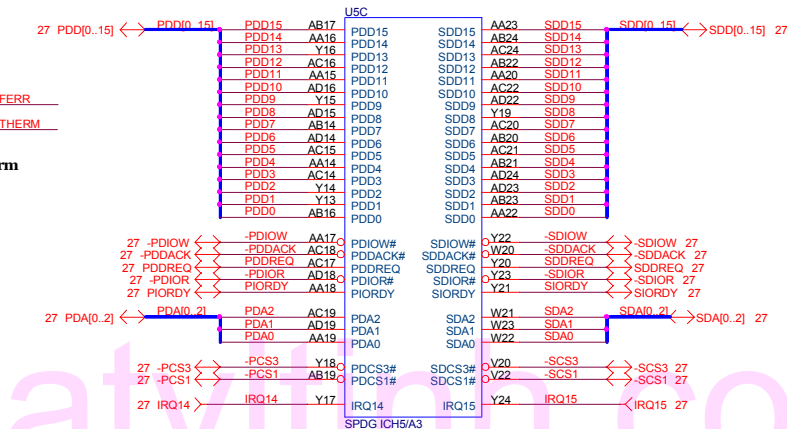


**CLR\_CMOS :**

1-2	CLEAR CMOS
2-3	NORMAL

**CLR\_PWD :**

OPEN	CLEAR PASSWORD
CLOSE	NORMAL



GIGABYTE CORP.

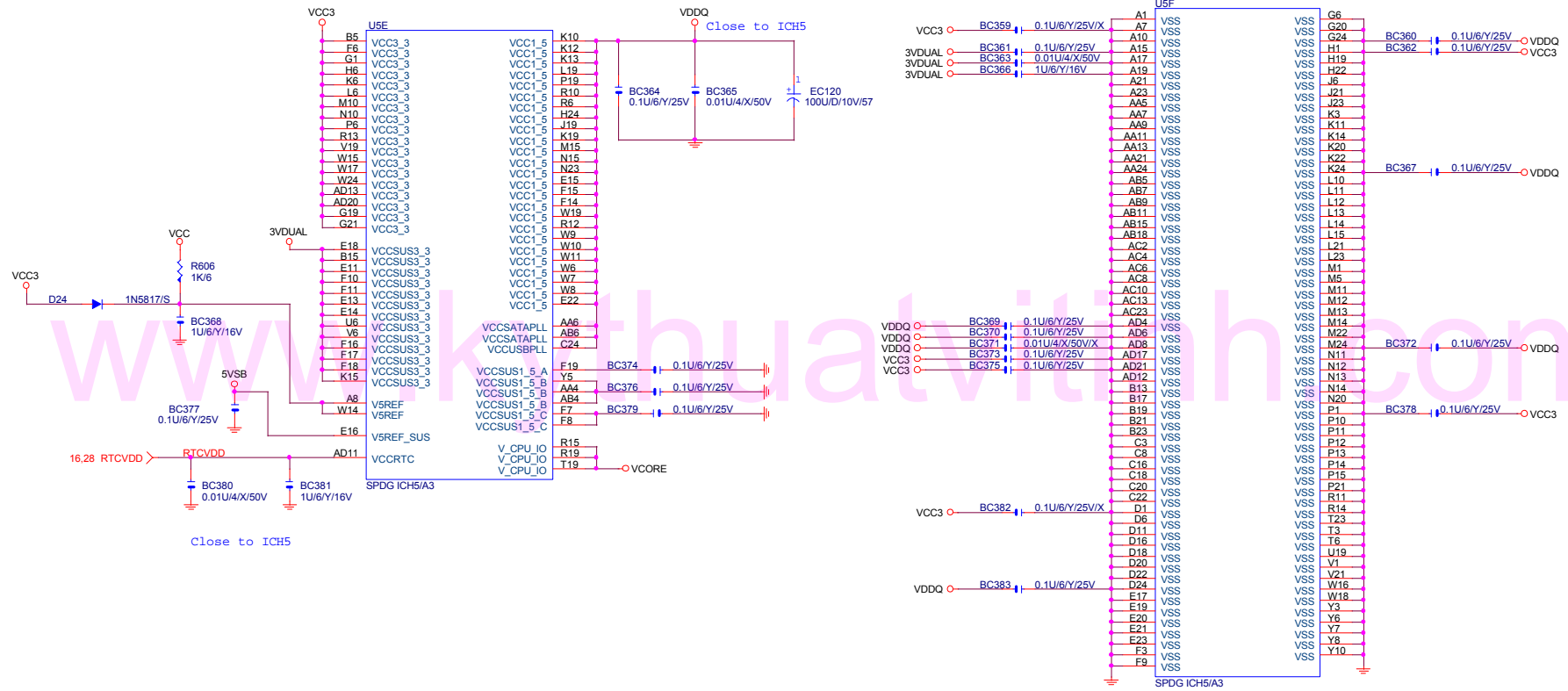
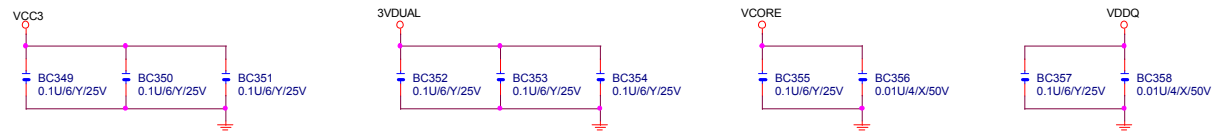
Title: **ICH5 IDE, GPIO, SATA, CTRL**

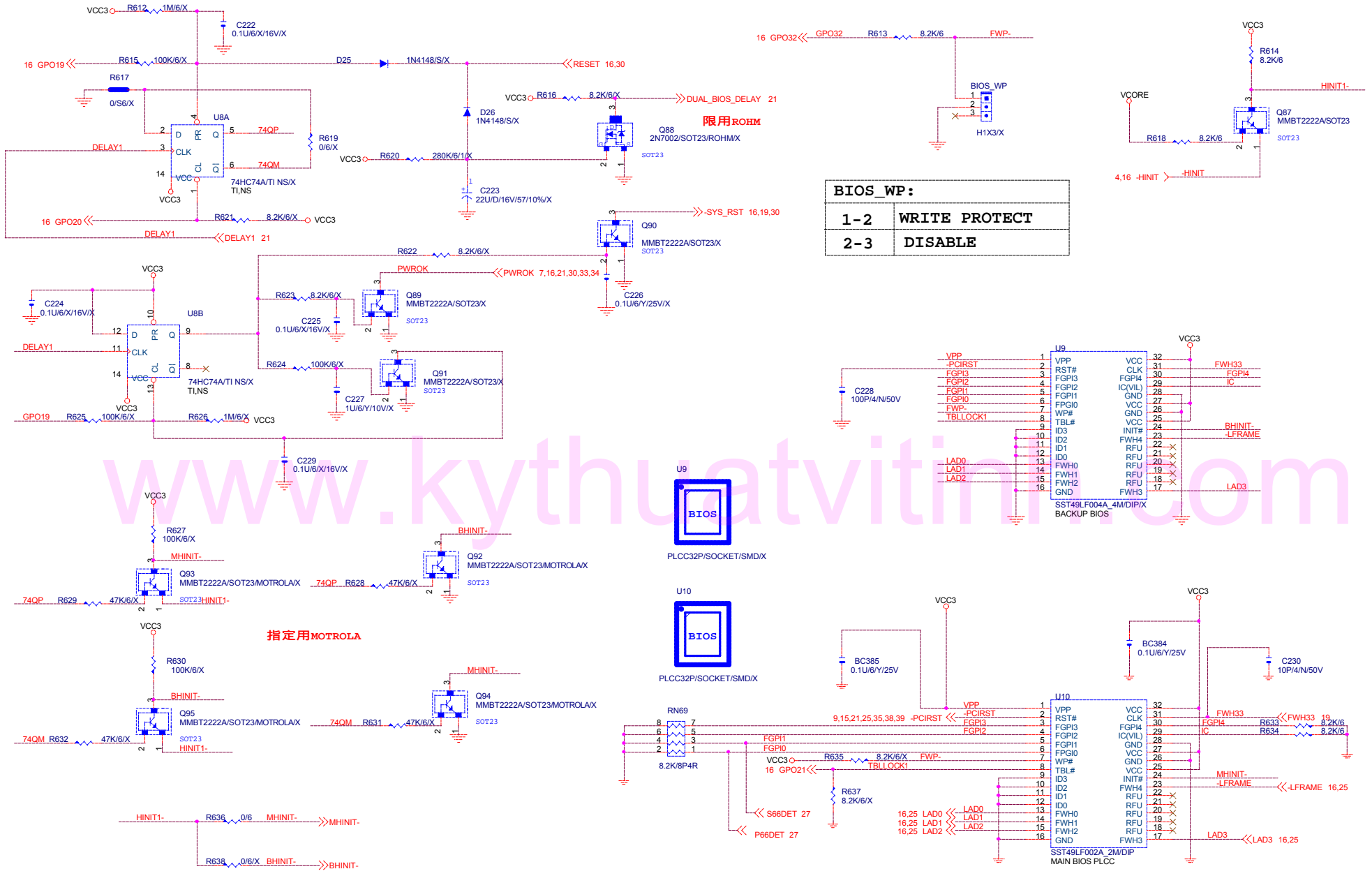
Size: **GA-8IP900**

Rev: **1.01**

Date: \_\_\_\_\_ Sheet 16 of 41

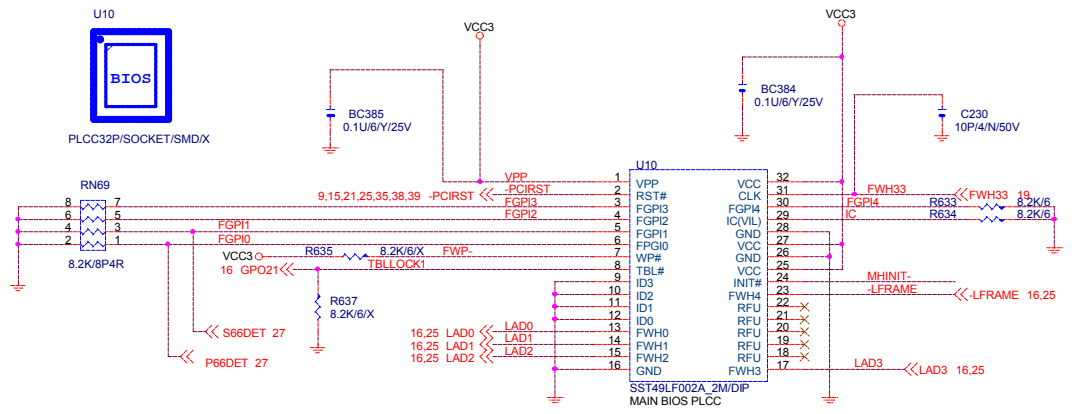
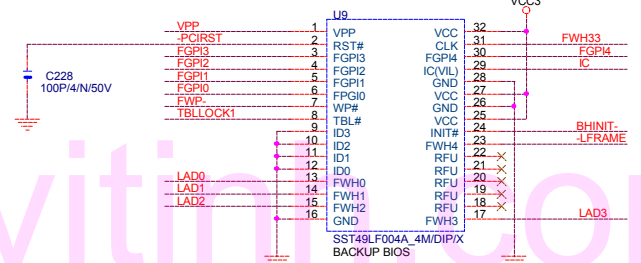






**BIOS\_WP:**

1-2	WRITE PROTECT
2-3	DISABLE



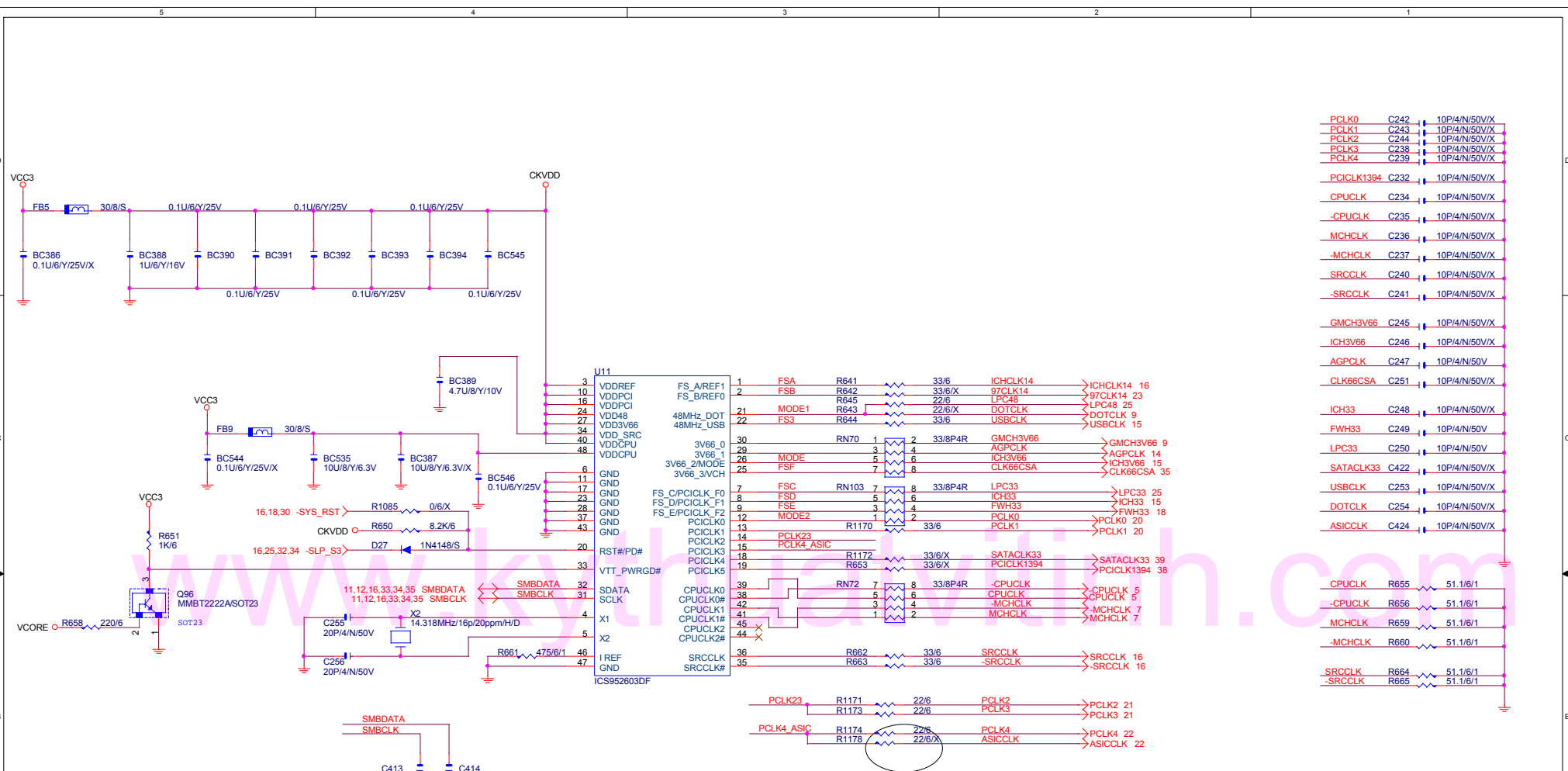
指定用MOTROLA

GIGABYTE CORP.

Title		
FWH		
Size	Document Number	Rev
B	GA-8IP900	1.0
Date:	Wednesday, April 16, 2003	Sheet 18 of 41

ADD WINBOUD FWH SEC. SOURCE

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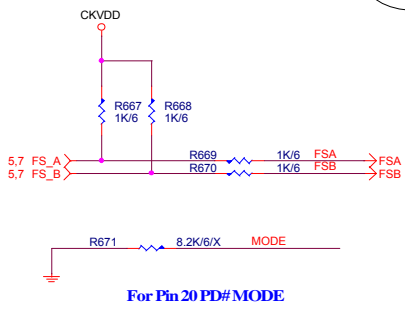
PCLK0	C242	10P/4/N/50V/X
PCLK1	C243	10P/4/N/50V/X
PCLK2	C244	10P/4/N/50V/X
PCLK3	C238	10P/4/N/50V/X
PCLK4	C239	10P/4/N/50V/X
PCCLK1394	C232	10P/4/N/50V/X
CPUCLK	C234	10P/4/N/50V/X
-CPUCLK	C235	10P/4/N/50V/X
MCHCLK	C236	10P/4/N/50V/X
-MCHCLK	C237	10P/4/N/50V/X
SRCCLK	C240	10P/4/N/50V/X
-SRCCLK	C241	10P/4/N/50V/X
GMCH3V66	C245	10P/4/N/50V/X
ICH3V66	C246	10P/4/N/50V/X
AGPCLK	C247	10P/4/N/50V
CLK66CSA	C251	10P/4/N/50V/X
ICH33	C248	10P/4/N/50V/X
FWH33	C249	10P/4/N/50V
LPC33	C250	10P/4/N/50V
SATACLK33	C422	10P/4/N/50V/X
USBCLK	C253	10P/4/N/50V/X
DOTCLK	C254	10P/4/N/50V/X
ASICCLK	C424	10P/4/N/50V/X
CPUCLK	R655	51.1/6/1
-CPUCLK	R656	51.1/6/1
MCHCLK	R659	51.1/6/1
-MCHCLK	R660	51.1/6/1
SRCCLK	R664	51.1/6/1
-SRCCLK	R665	51.1/6/1

**CYPRESS CY28405**

FS_E	FS_D	FS_C	FS_B	FS_A	Clock
1	1	0	0	0	100.9MHz
1	1	0	0	1	133.9MHz
1	1	0	1	1	166.9MHz
1	1	0	1	0	200.9MHz

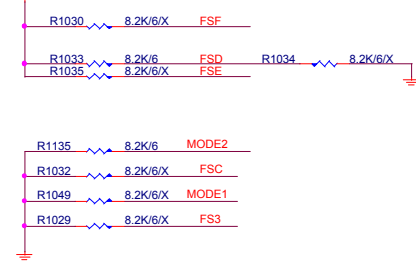
**ICS952616**

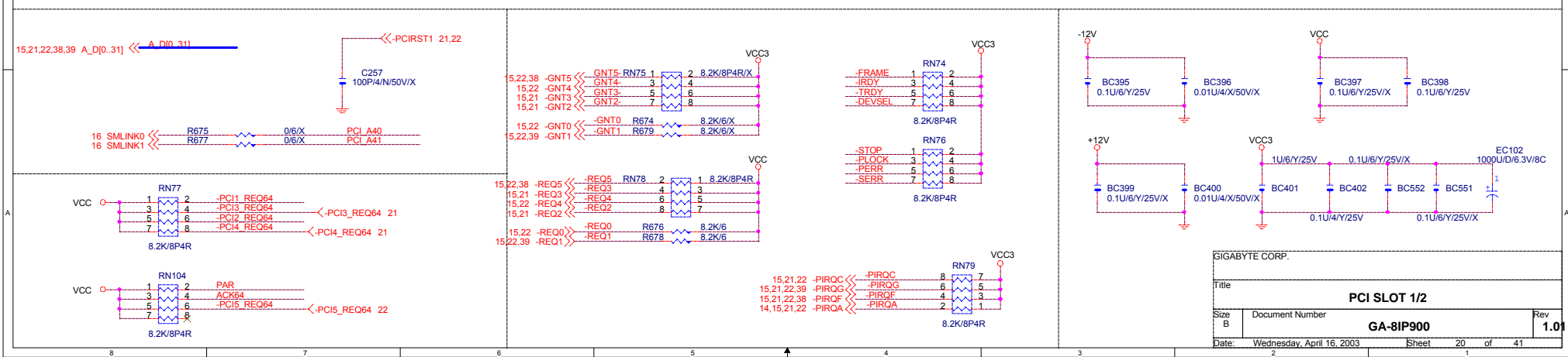
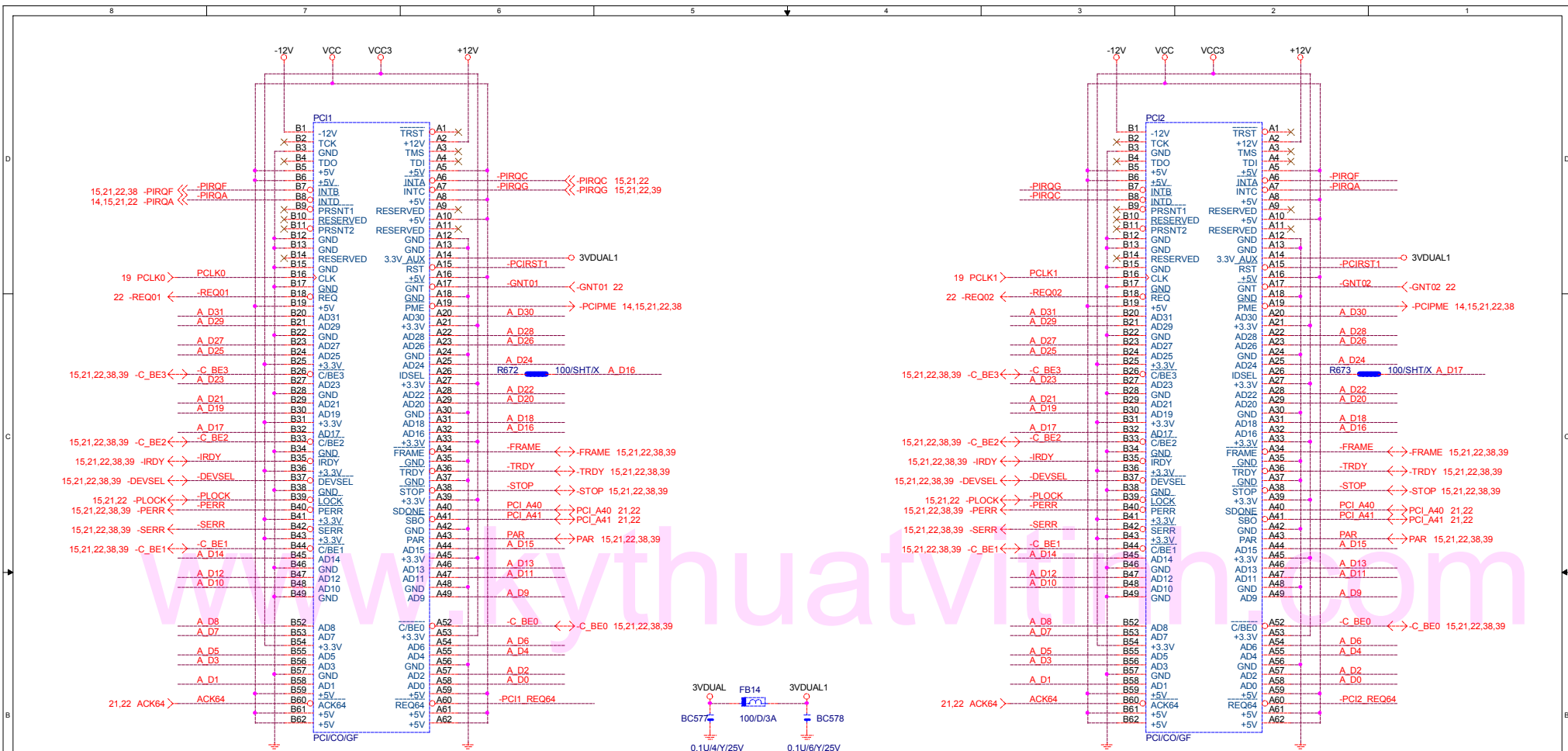
FS_E	FS_3	FS_C	FS_B	FS_A	Clock
1	0	0	0	0	100MHz
1	0	0	0	1	133MHz
1	0	0	1	1	166MHz
1	0	0	1	0	200MHz



For Pin 20 PD# MODE

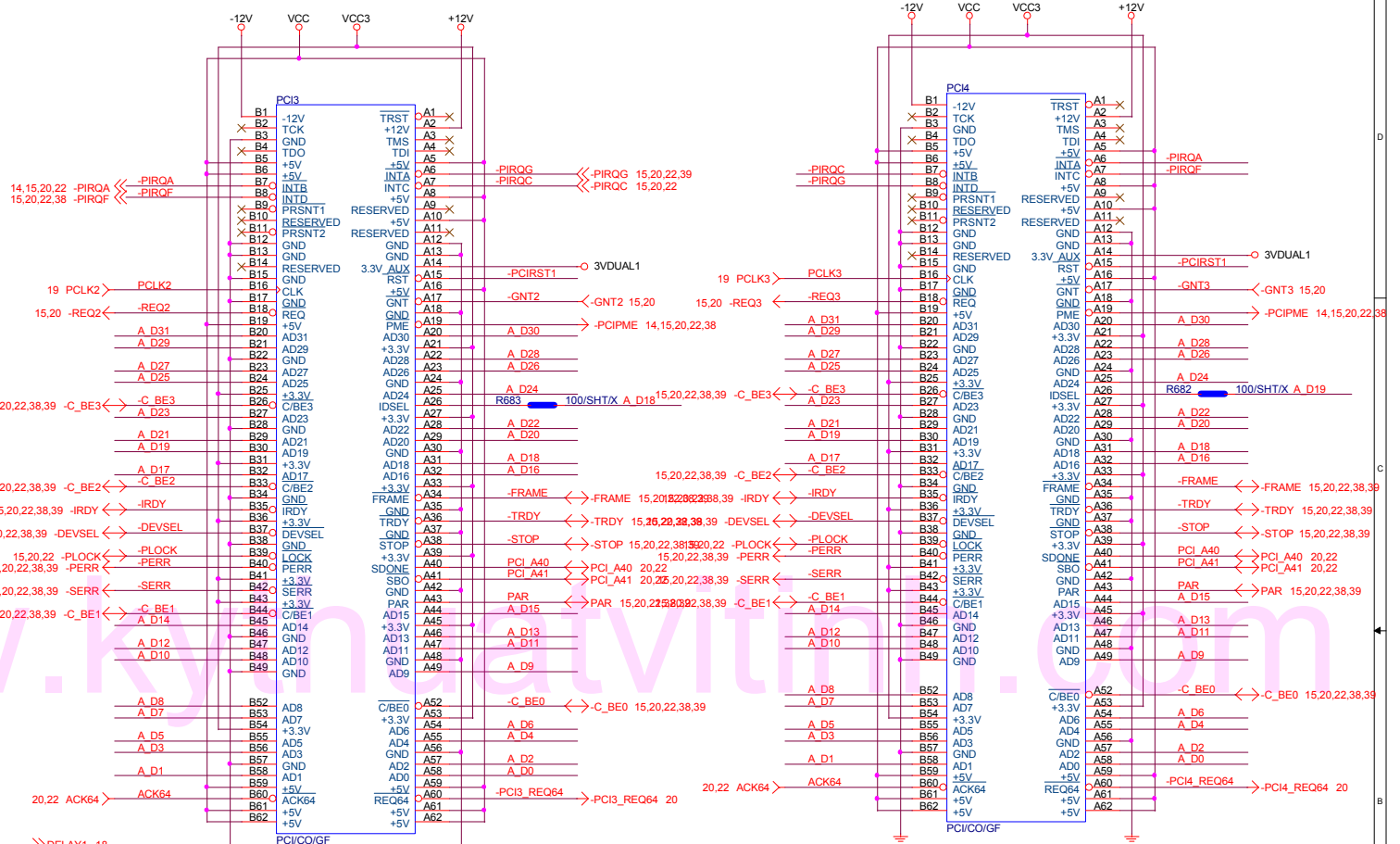
**ICS + CYPRESS CO-LAYOUT**



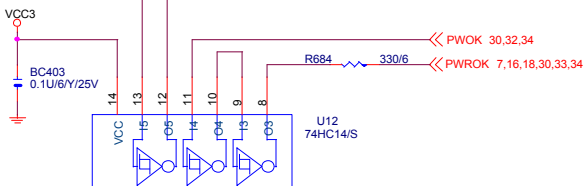


GIGABYTE CORP.		
Title <b>PCI SLOT 1/2</b>		
Size B	Document Number <b>GA-8IP900</b>	Rev <b>1.01</b>
Date: Wednesday, April 16, 2003	Sheet 20	of 41

15,20,22,38,39 A\_D[0..31] << A\_D[0..31]



18 DUAL\_BIOS\_DELAY << DELAY1 18



9,15,18,25,35,38,39 -PCIRST << PCIRST- FROM ICH5

18 DUAL\_BIOS\_DELAY << DELAY1 18

VCC3

BC403 0.1uF/25V

R684 330/6 << PWOK 30,32,34

<< PWROK 7,16,18,30,33,34

U12 74HC14/S

<< -AGPRST 14 TO AGP SLOT

-AGPRST

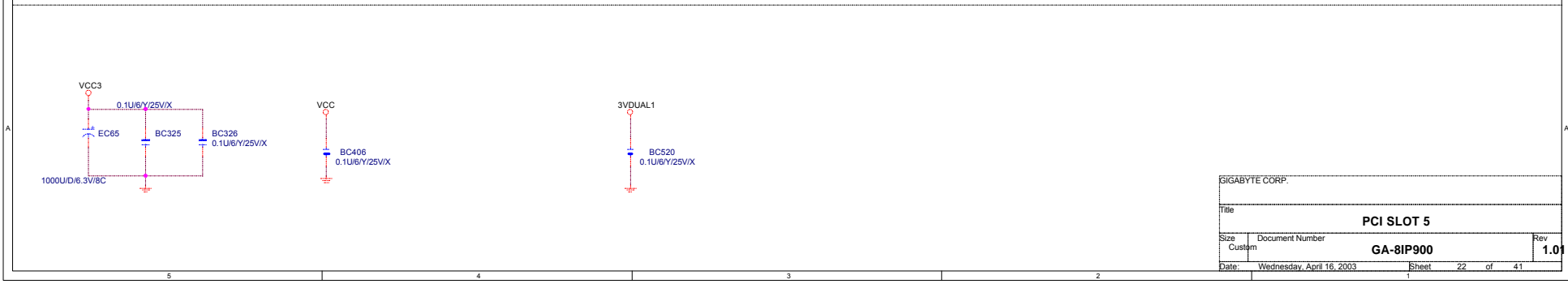
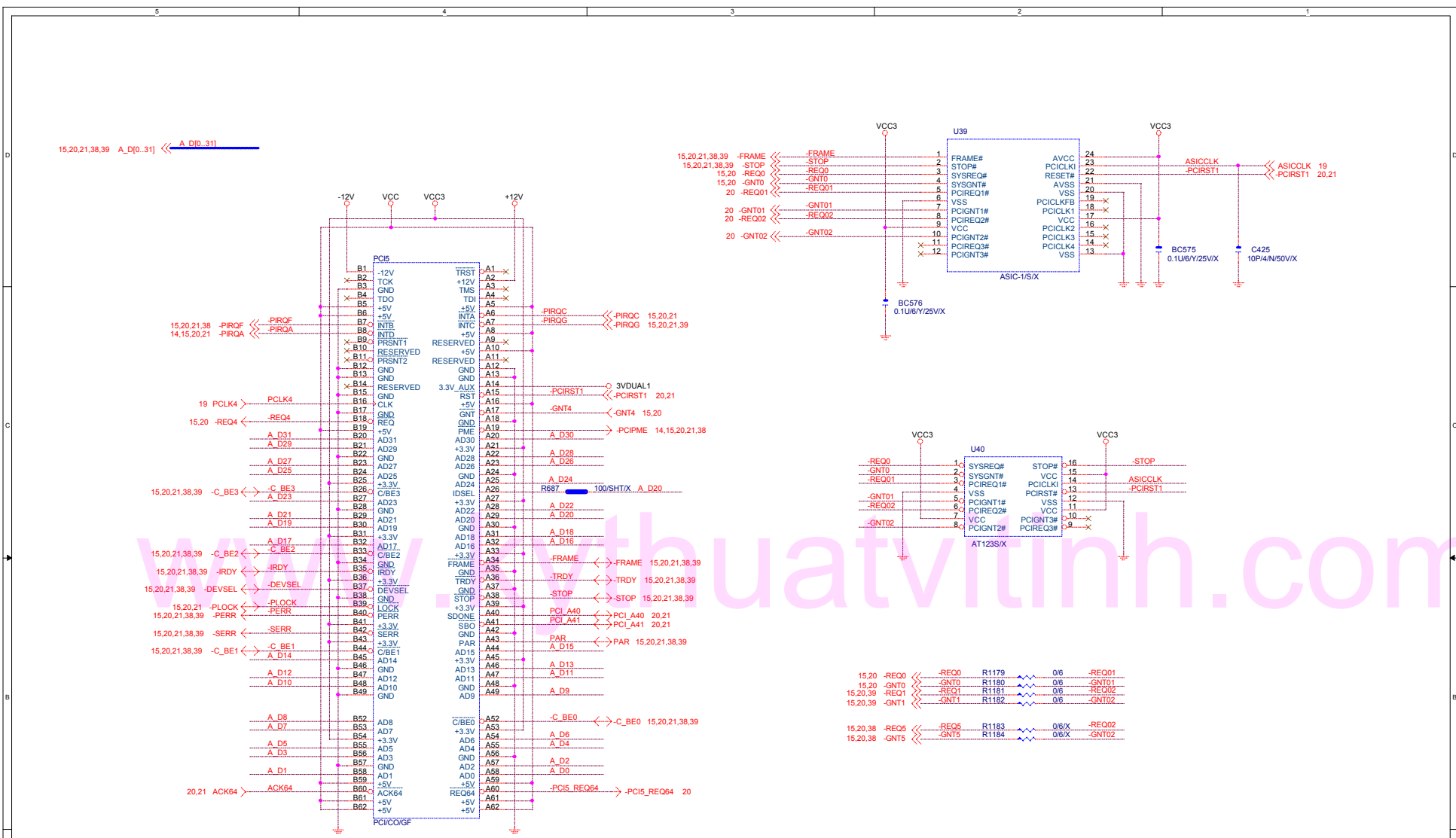
<< -PCIRST1 20,22 TO PCI SLOT

-PCIRST1

<< -IDERST 27 TO IDE SLOT

-IDERST

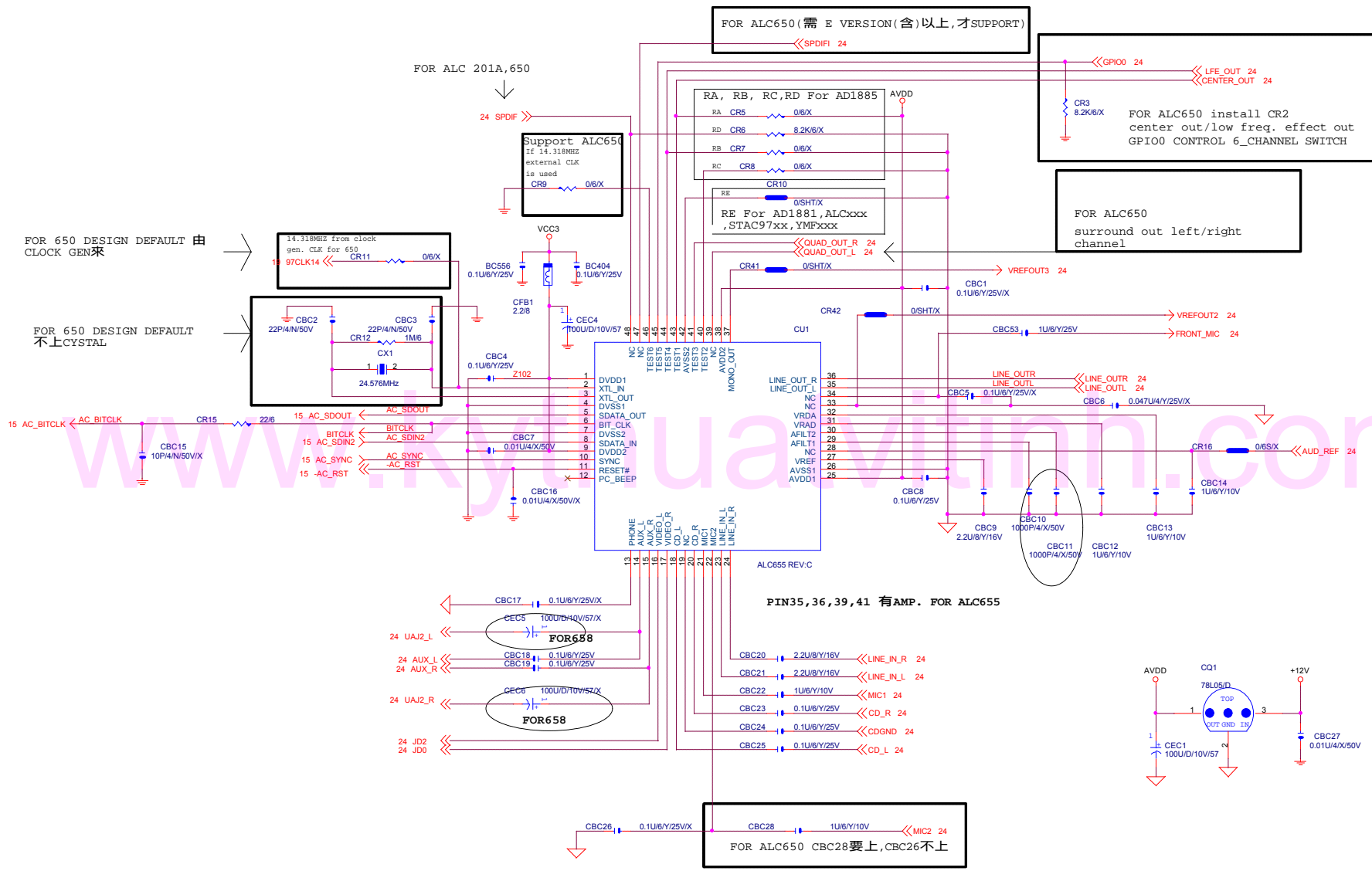
GIGABYTE CORP.		
Title		
PCI SLOT 3/4		
Size	Document Number	Rev
B	GA-8IP900	1.0
Date:	Wednesday, April 16, 2003	Sheet 21 of 41



SIGNAL			
15.20.21.38.39	-FRAME	<<	-FRAME
15.20.21.38.39	-STOP	<<	-STOP
15.20	-REQ0	<<	-REQ0
15.20	-GNT0	<<	-GNT0
20	-REQ1	<<	-REQ1
20	-GNT1	<<	-GNT1
20	-REQ2	<<	-REQ2
20	-GNT2	<<	-GNT2
19	PCLK4	<<	PCLK4
15.20	-REQ4	<<	-REQ4
15.20.21.38.39	-C_BE3	<<	-C_BE3
15.20.21.38.39	-C_BE2	<<	-C_BE2
15.20.21.38.39	-C_BE1	<<	-C_BE1
15.20.21.38.39	-C_BE0	<<	-C_BE0
20.21	ACK64	<<	ACK64
15.20	-REQ0	<<	-REQ0
15.20	-GNT0	<<	-GNT0
15.20.39	-REQ1	<<	-REQ1
15.20.39	-GNT1	<<	-GNT1
15.20.38	-REQ5	<<	-REQ5
15.20.38	-GNT5	<<	-GNT5

POWER			
VCC3	0.1uF/6Y25V/X	BC576	0.1uF/6Y25V/X
VCC	0.1uF/6Y25V/X	BC406	0.1uF/6Y25V/X
3VDUAL1	0.1uF/6Y25V/X	BC520	0.1uF/6Y25V/X

SIGNAL			
15.20	-REQ0	R1179	0/6 -REQ0
15.20	-GNT0	R1180	0/6 -GNT0
15.20.39	-REQ1	R1181	0/6 -REQ1
15.20.39	-GNT1	R1182	0/6 -GNT1
15.20.38	-REQ5	R1183	0/6X -REQ5
15.20.38	-GNT5	R1184	0/6X -GNT5

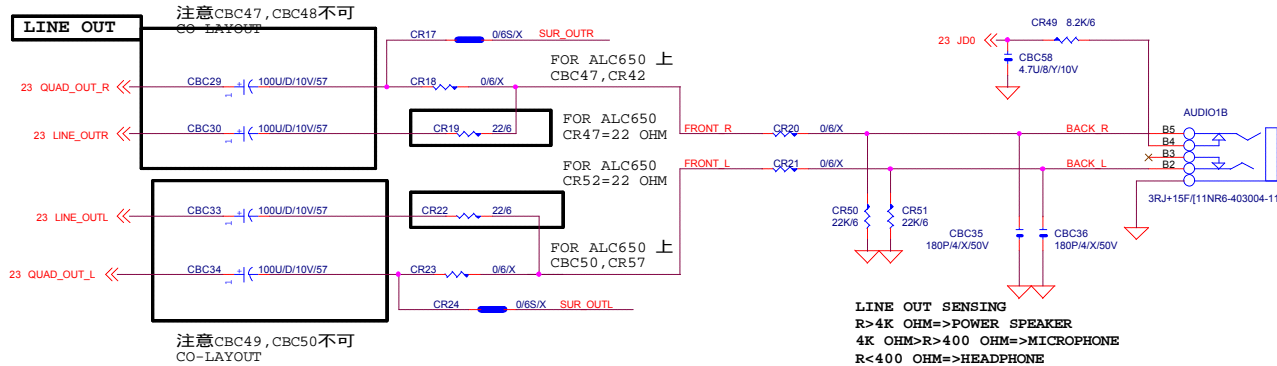


SIGABYTE CORP.			
Title			
ALC655			
Size	Document Number		Rev
Custom	GA-8IP900		1.01
Date:	Wednesday, April 16, 2003	Sheet	23 of 41



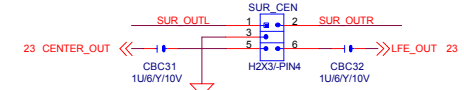
JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual)

1/2(3.14)RC=1/2(3.14)8.2K\*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav )



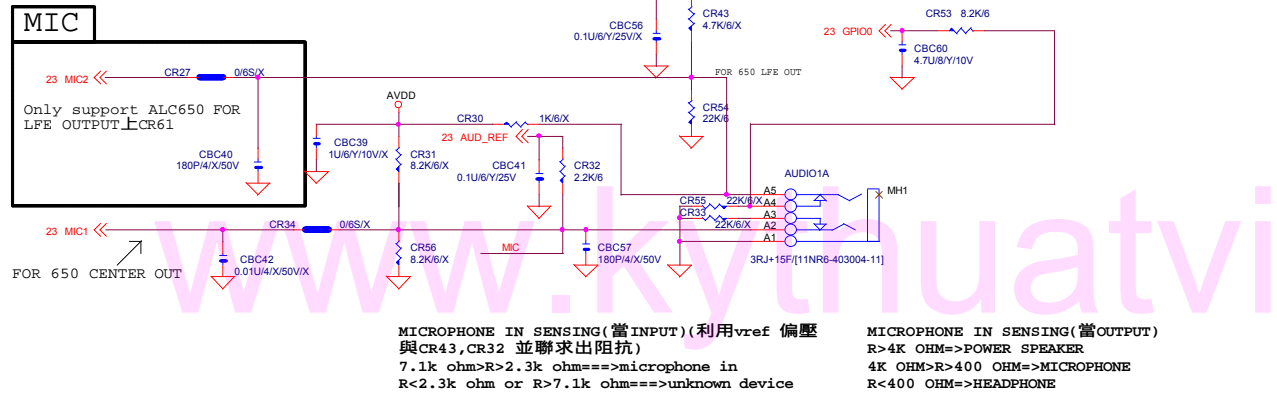
FOR SUPPORT 6 CHANNEL,  
SURROUND OUT

CENTER OUT, LOW  
FREQUENCY EFFECT OUT

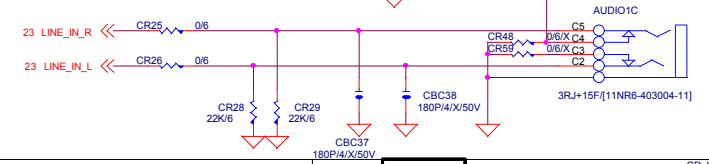


LINE IN SENSING(當OUTPUT)  
R>4K OHM=>POWER SPEAKER  
4K OHM>R>400 OHM=>MICROPHONE  
R<400 OHM=>HEADPHONE

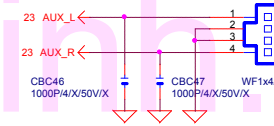
LINE IN SENSING(當INPUT)  
swing of input signal>-40dbv(10mv)====>line in device active  
swing of input signal<-40dbv(10mv)====>unknown line in device



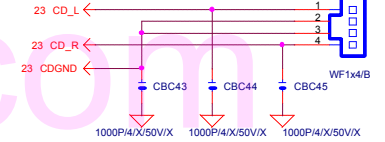
LINE-IN



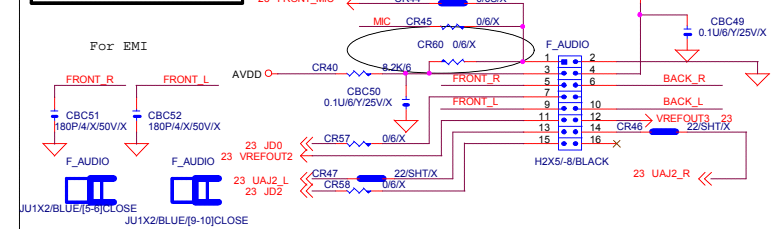
AUX IN DEFAULT NO POP



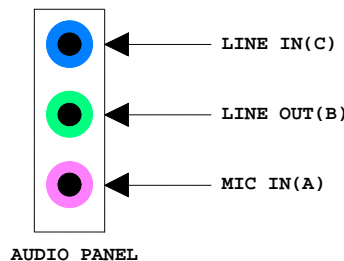
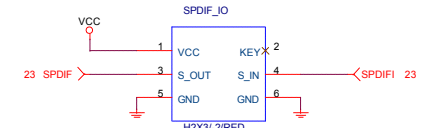
CD IN



INTEL FRONT AUDIO

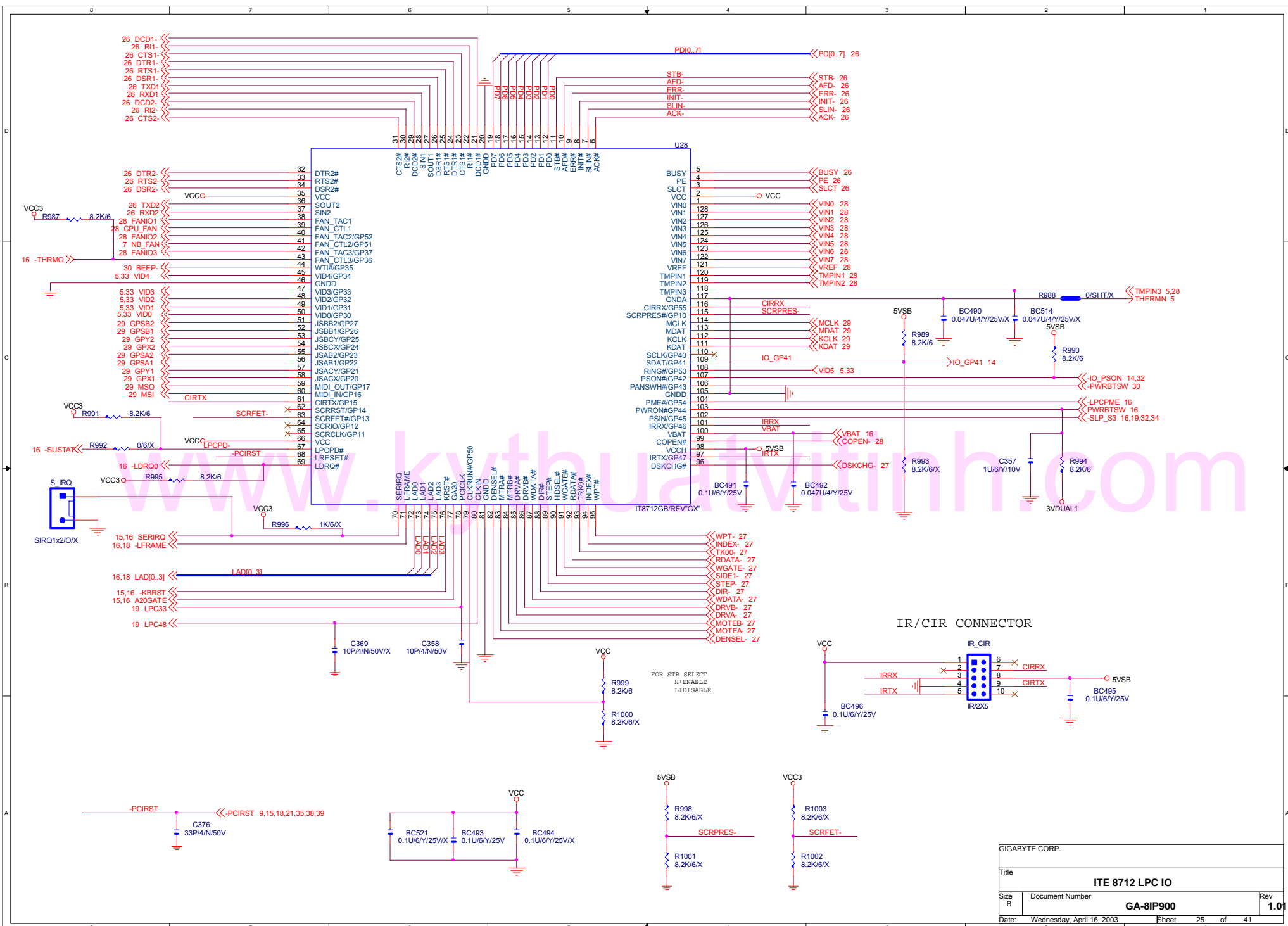


SPDIF

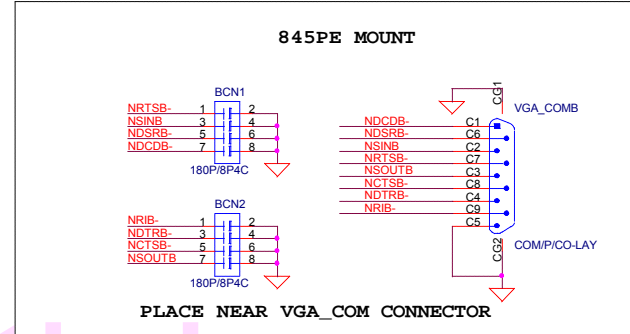
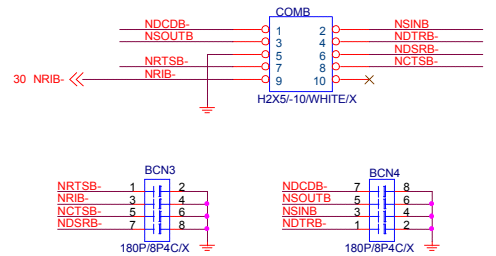
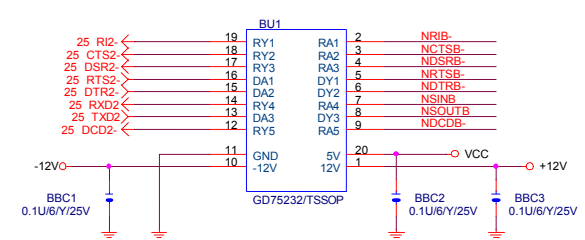
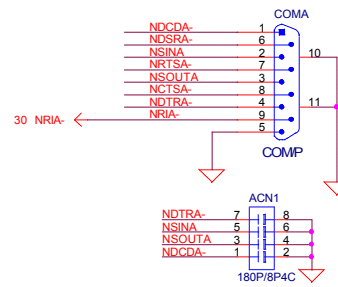
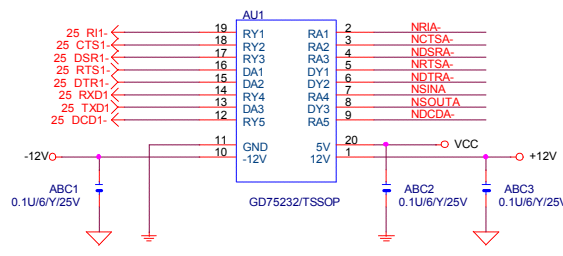


<b>GIGABYTE CORP.</b>			
<b>AUDIO OUTPUT, GAME PORT</b>			
Title	Document Number		Rev
Size	GA-8IP900		1.01
Custom			
Date	Wednesday, April 16, 2003	Sheet	24 of 41

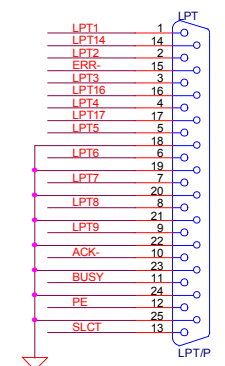
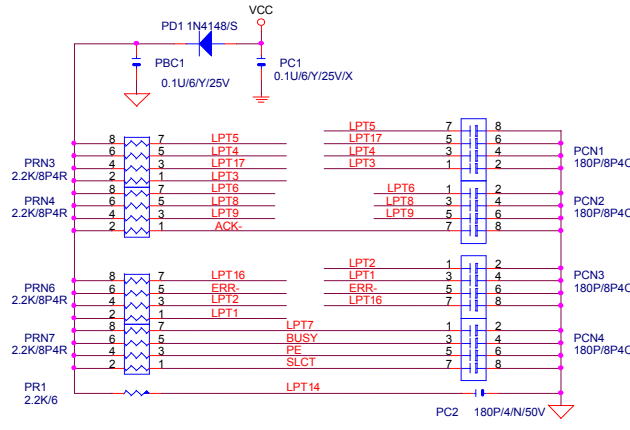
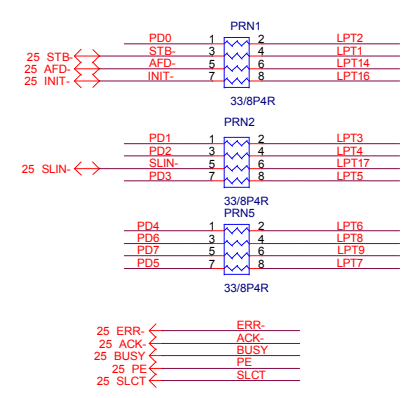


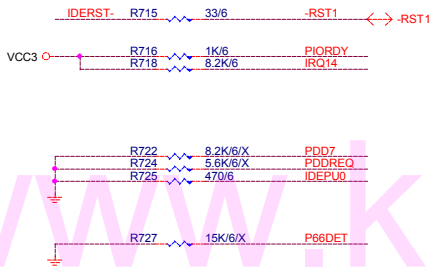
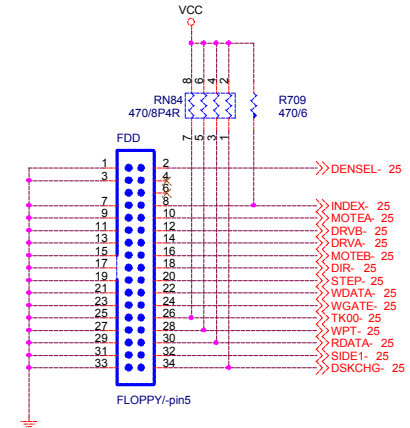
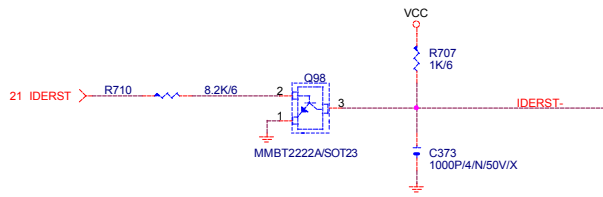


GIGABYTE CORP.		
Title		
<b>ITE 8712 LPC IO</b>		
Size	Document Number	Rev
B	<b>GA-8IP900</b>	<b>1.01</b>
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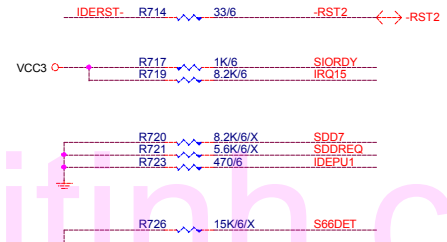


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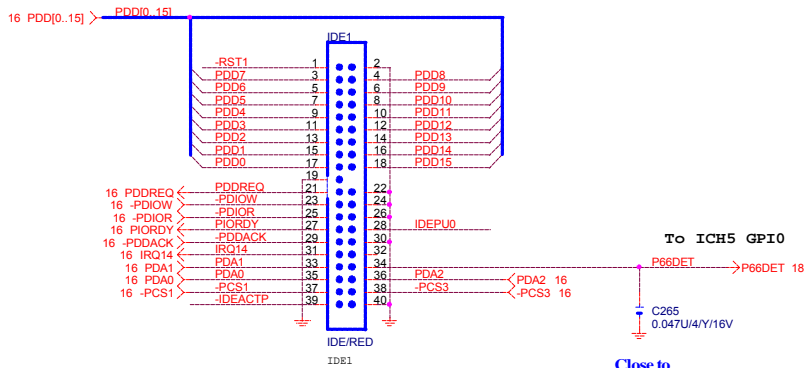




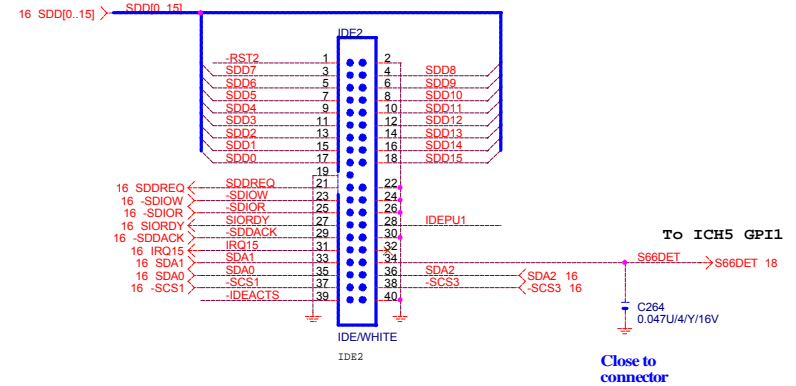
PRIMARY IDE CONNECTOR



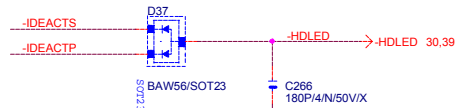
SECONDARY IDE CONNECTOR



Close to connector



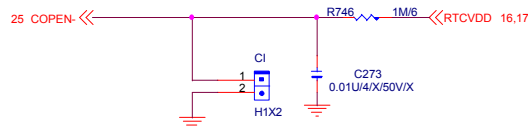
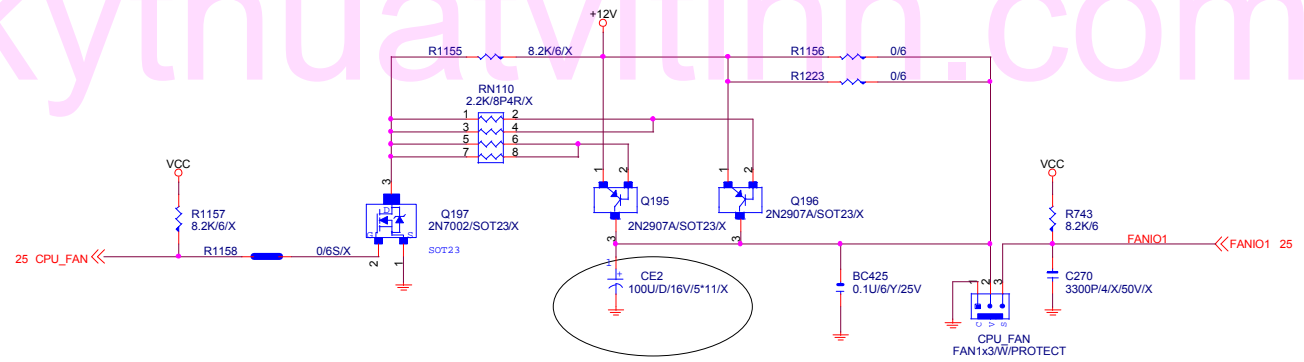
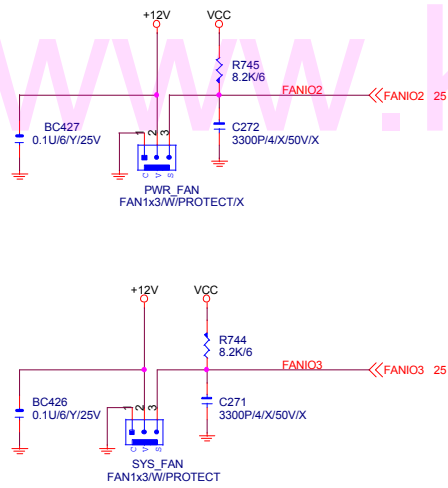
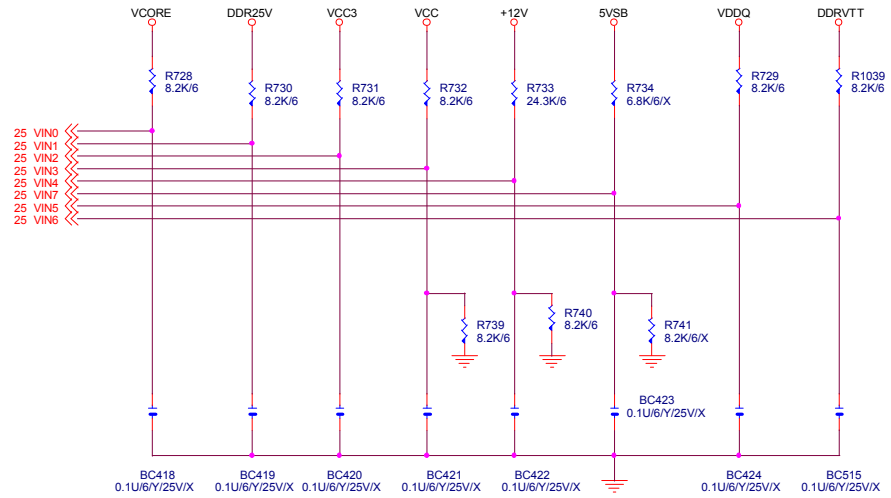
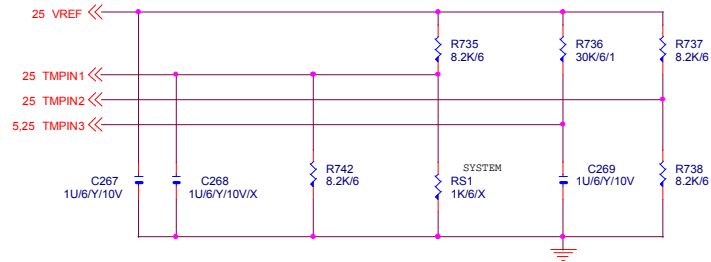
Close to connector



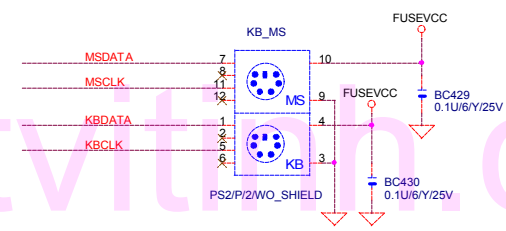
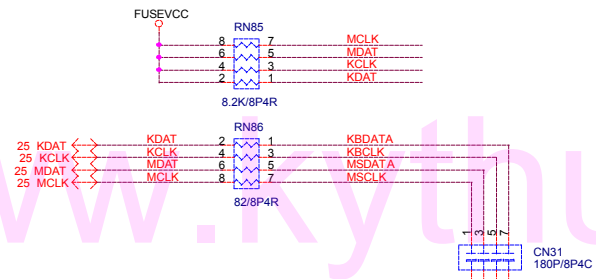
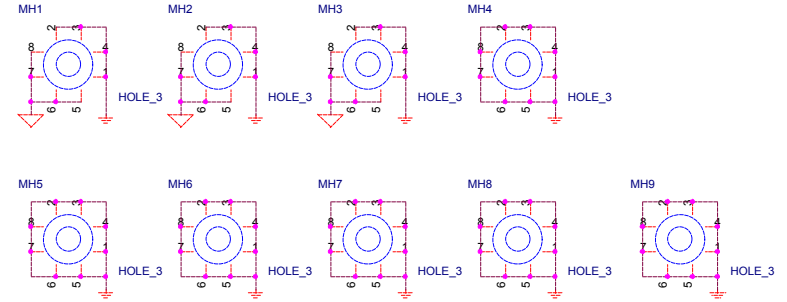
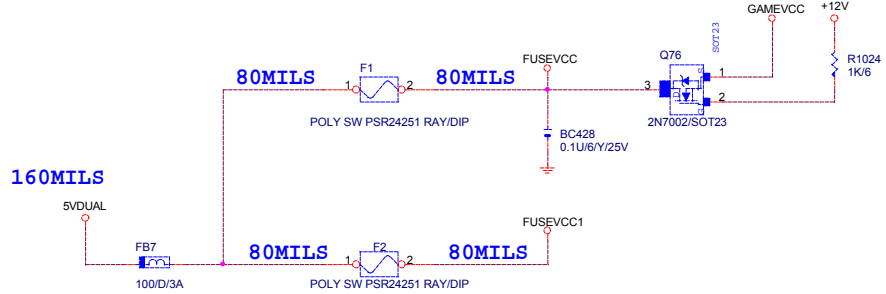
GIGABYTE CORP.

Title		
<b>IDE CONNECTOR</b>		
Size B	Document Number	Rev
	<b>GA-8IP900</b>	<b>1.01</b>
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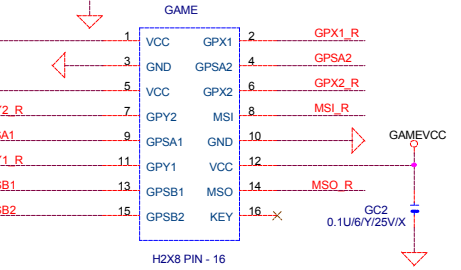
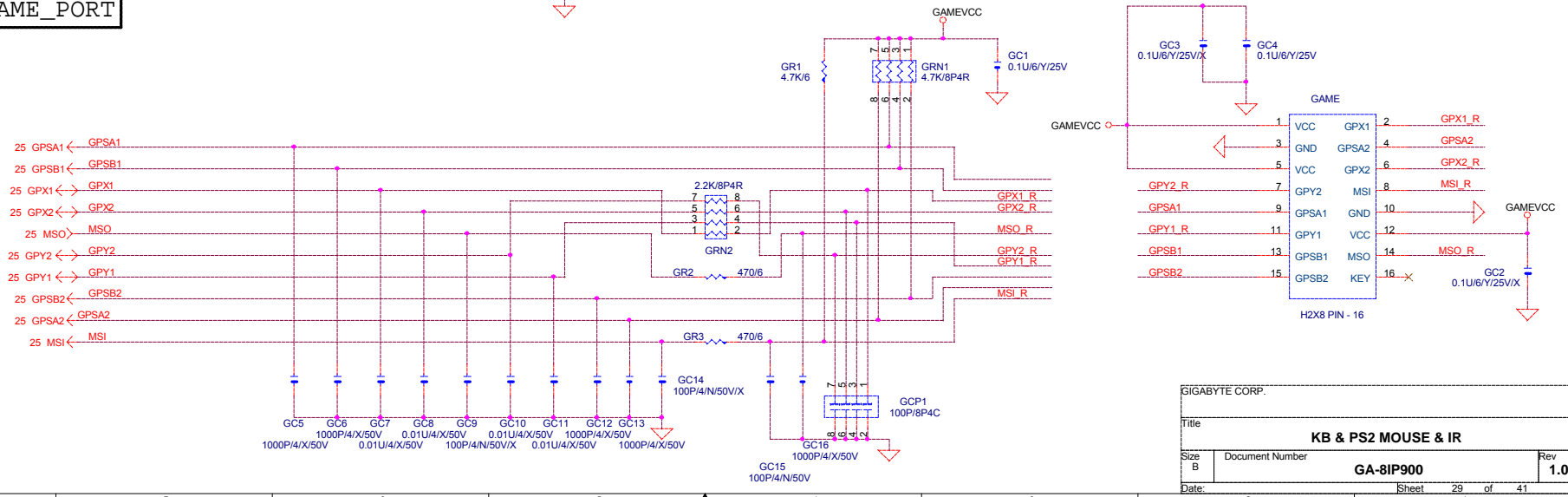
# Hardware Monitor circuits



GIGABYTE CORP.		
Title		
<b>FAN/HWMO</b>		
Size B	Document Number	Rev
	<b>GA-8IP900</b>	<b>1.01</b>
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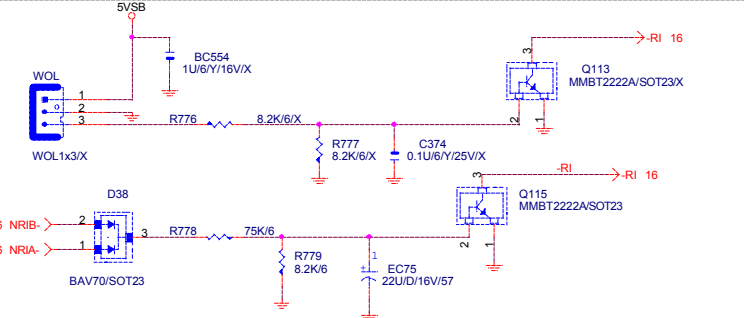
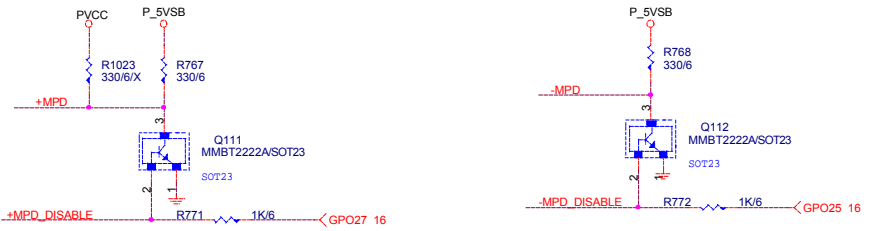
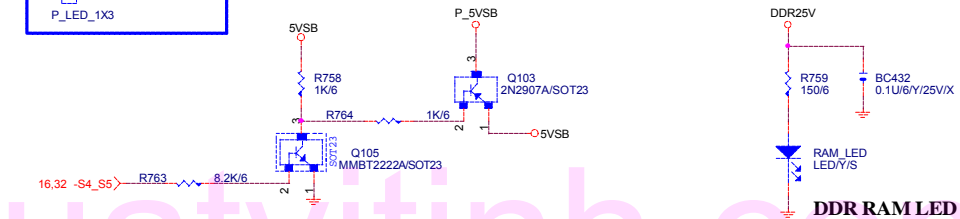
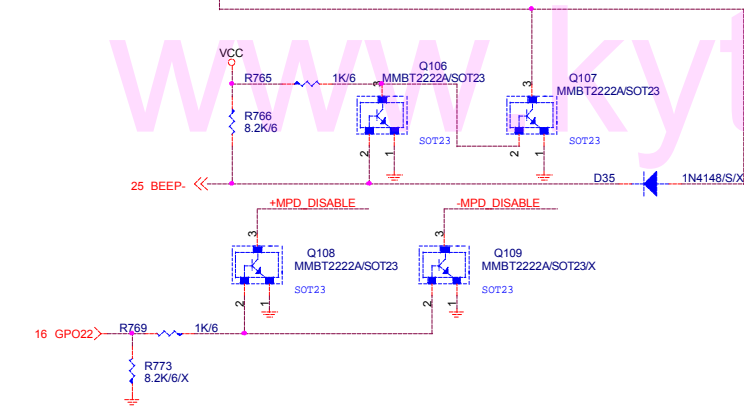
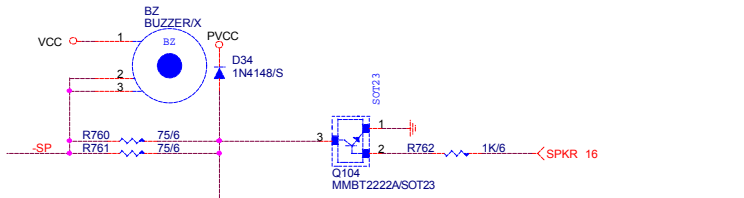
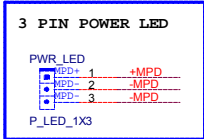
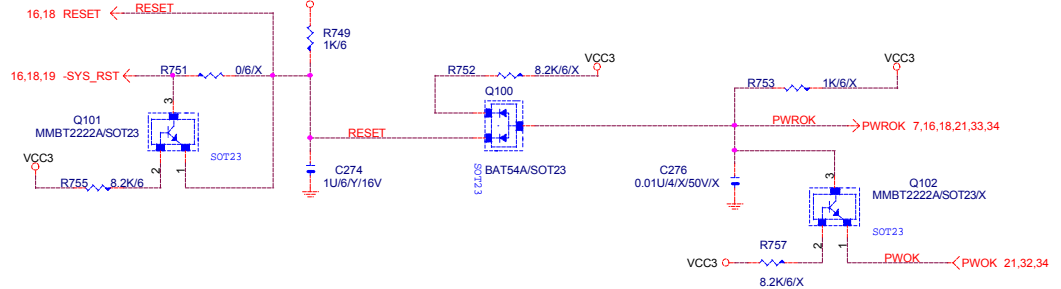
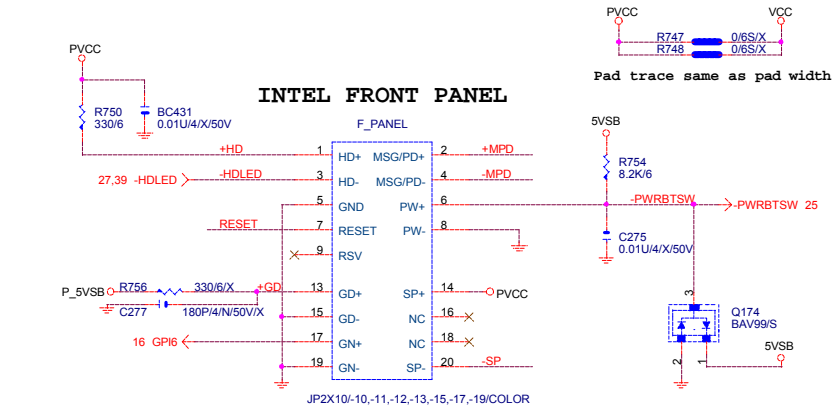


GAME\_PORT



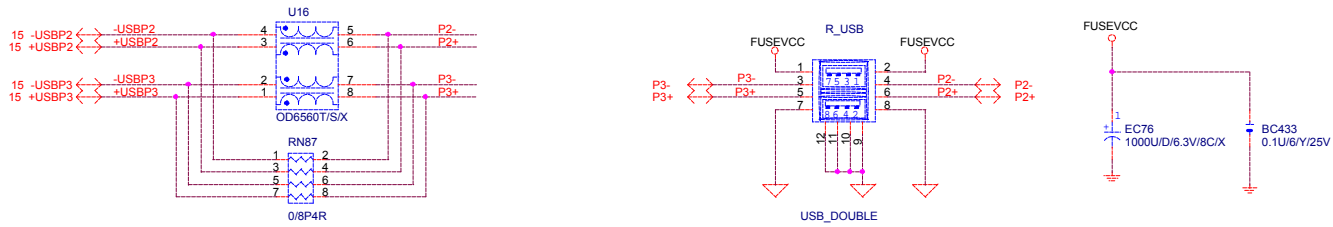
GIGABYTE CORP.		
Title		
<b>KB &amp; PS2 MOUSE &amp; IR</b>		
Size	Document Number	Rev
B	<b>GA-8IP900</b>	<b>1.01</b>
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### INTEL FRONT PANEL

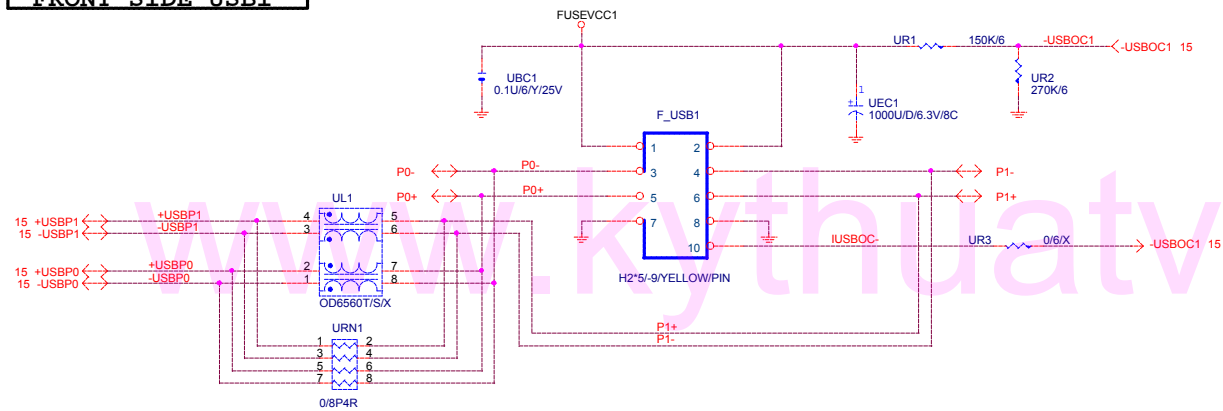


GIGABYTE CORP.		
Title		
<b>PANEL &amp; STR LED &amp; RI</b>		
Size B	Document Number	Rev
	<b>GA-8IP900</b>	<b>1.01</b>
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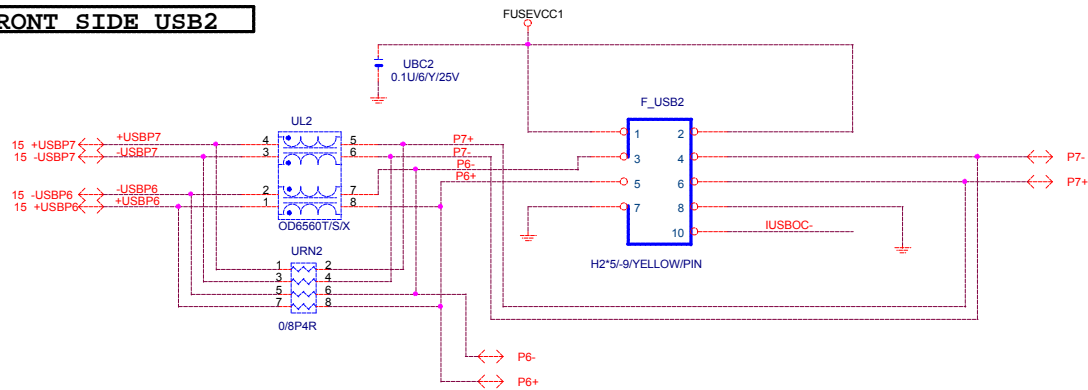
# REAR USB



# FRONT SIDE USB1



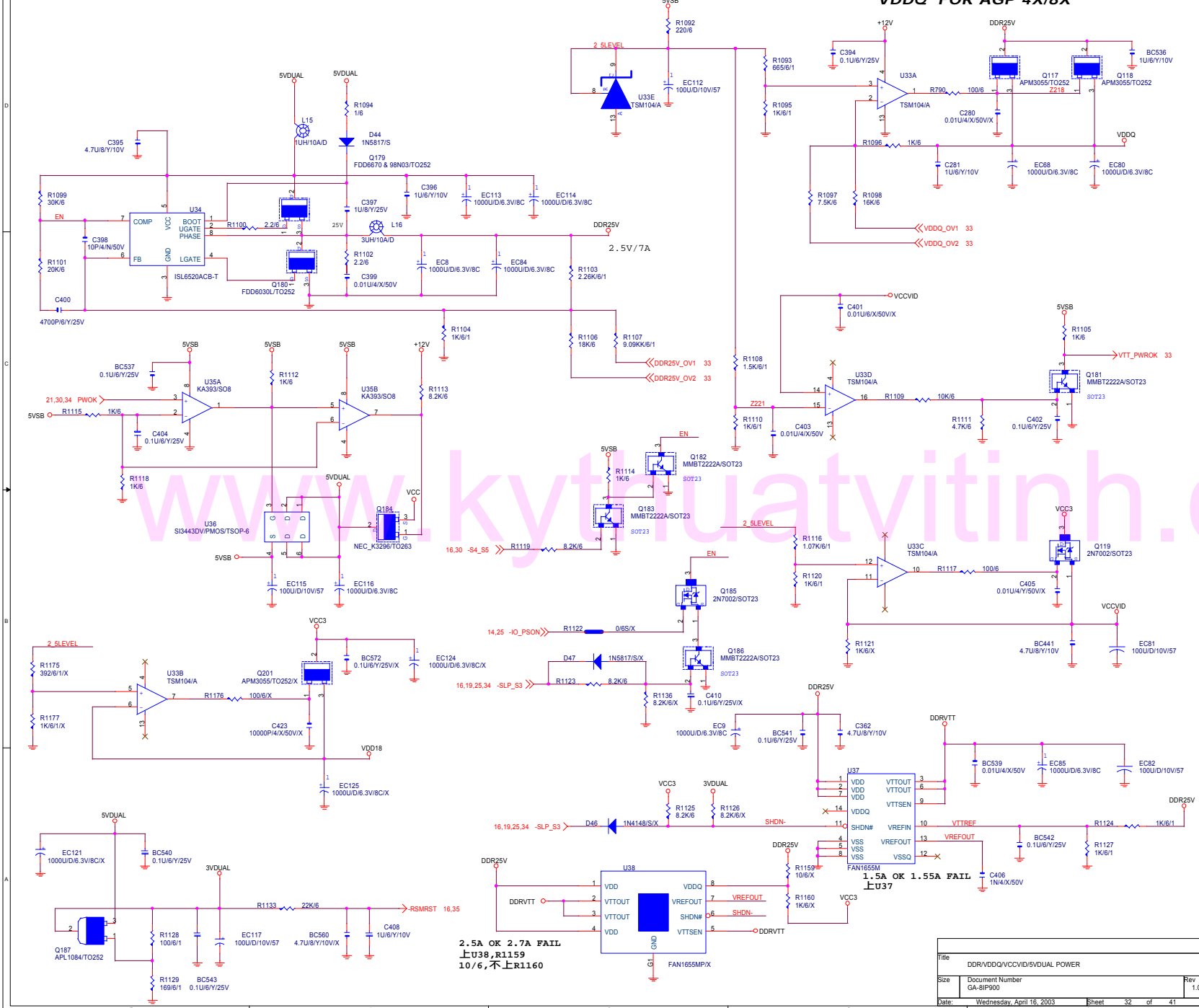
# FRONT SIDE USB2



GIGABYTE CORP.		
Title		
<b>ICH USB PORT</b>		
Size B	Document Number	Rev
	<b>GA-8IP900</b>	<b>1.01</b>
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**DDR25V FOR DDR DIMM & NB**

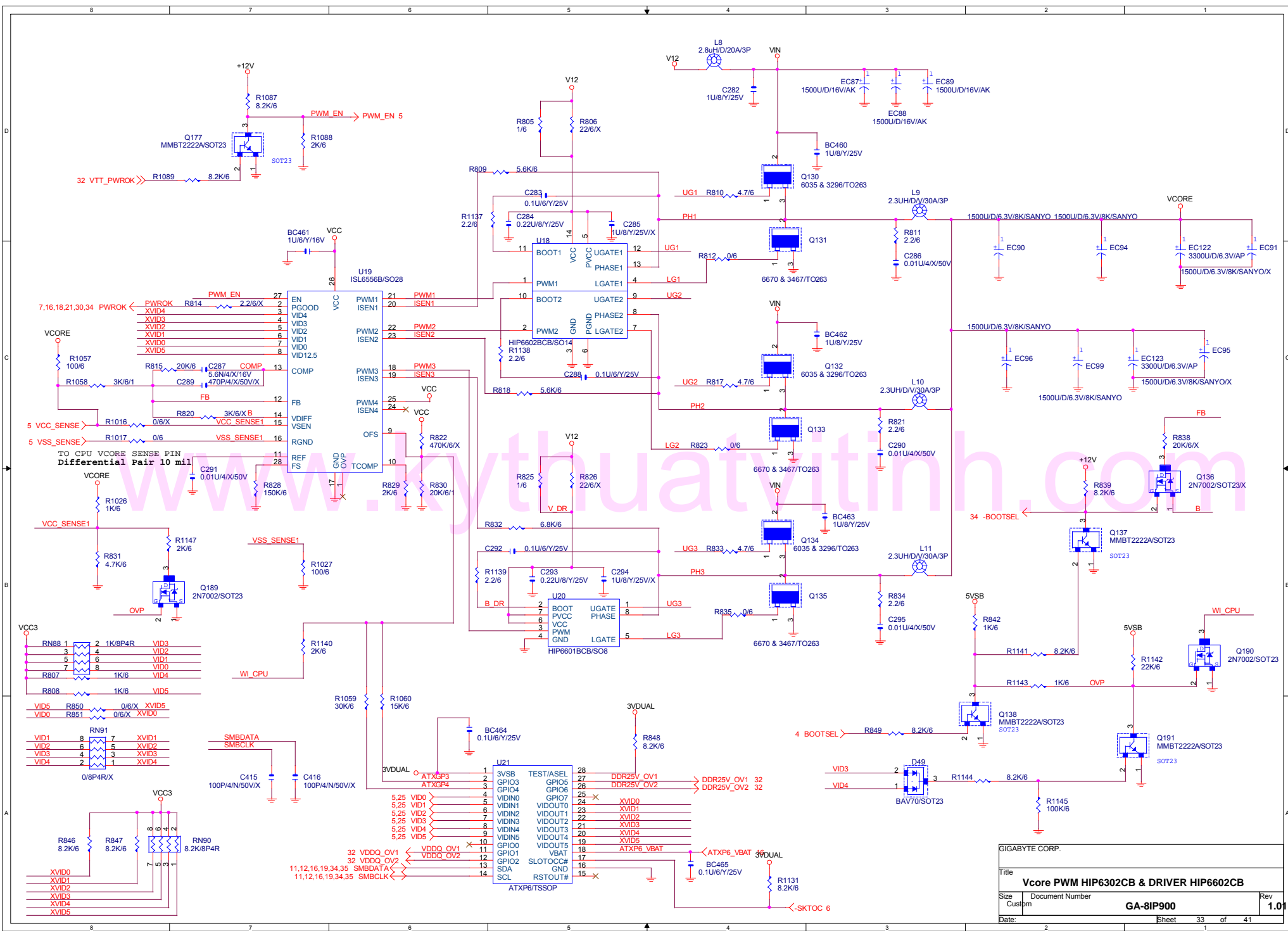
**VDDQ FOR AGP 4X/8X**



2.5A OK 2.7A FAIL  
 U38, R1159  
 10/6, 不上R1160

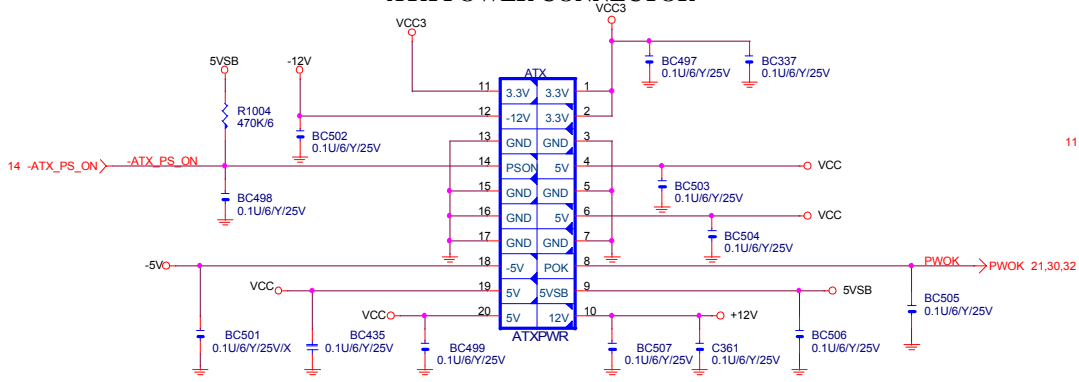
File		
DDR/VDDQ/VCCVID/5VDUAL POWER		
Size	Document Number	Rev
	GA-8IP900	1.01
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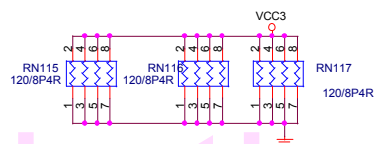
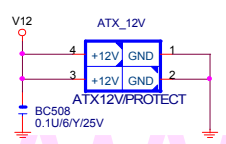
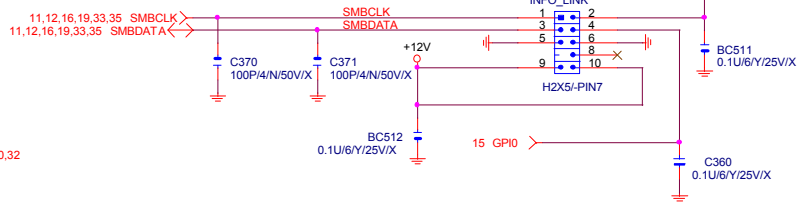


GIGABYTE CORP.		
Title	Vcore PWM HIP6302CB & DRIVER HIP6602CB	
Size	Document Number	Rev
Custom	GA-8IP900	1.01
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# ATX POWER CONNECTOR

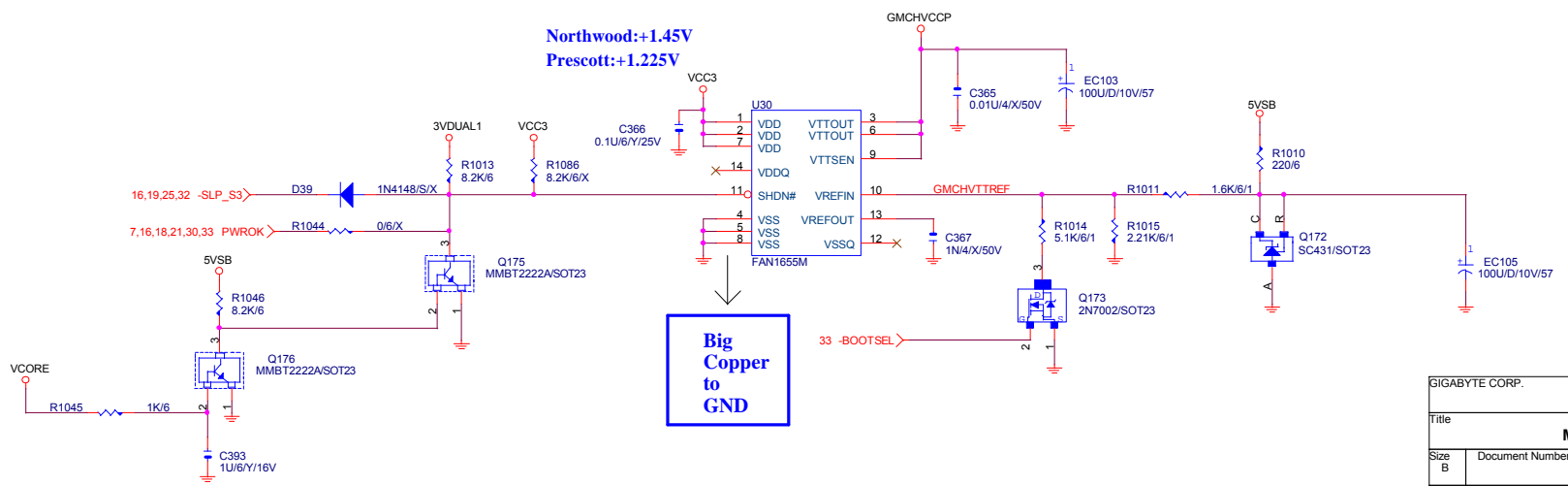


# SMBUS CONN.



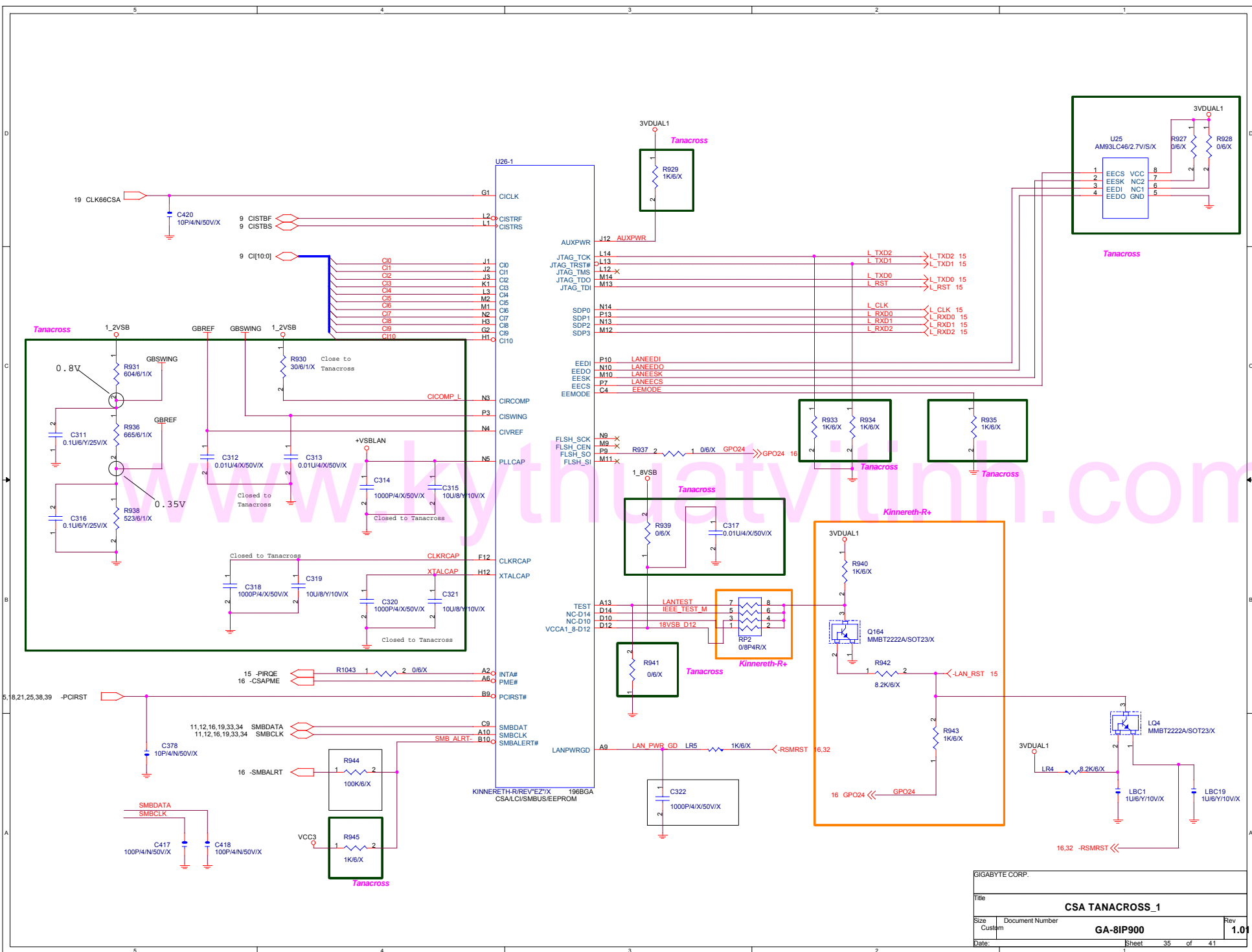
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Northwood:+1.45V  
Prescott:+1.225V

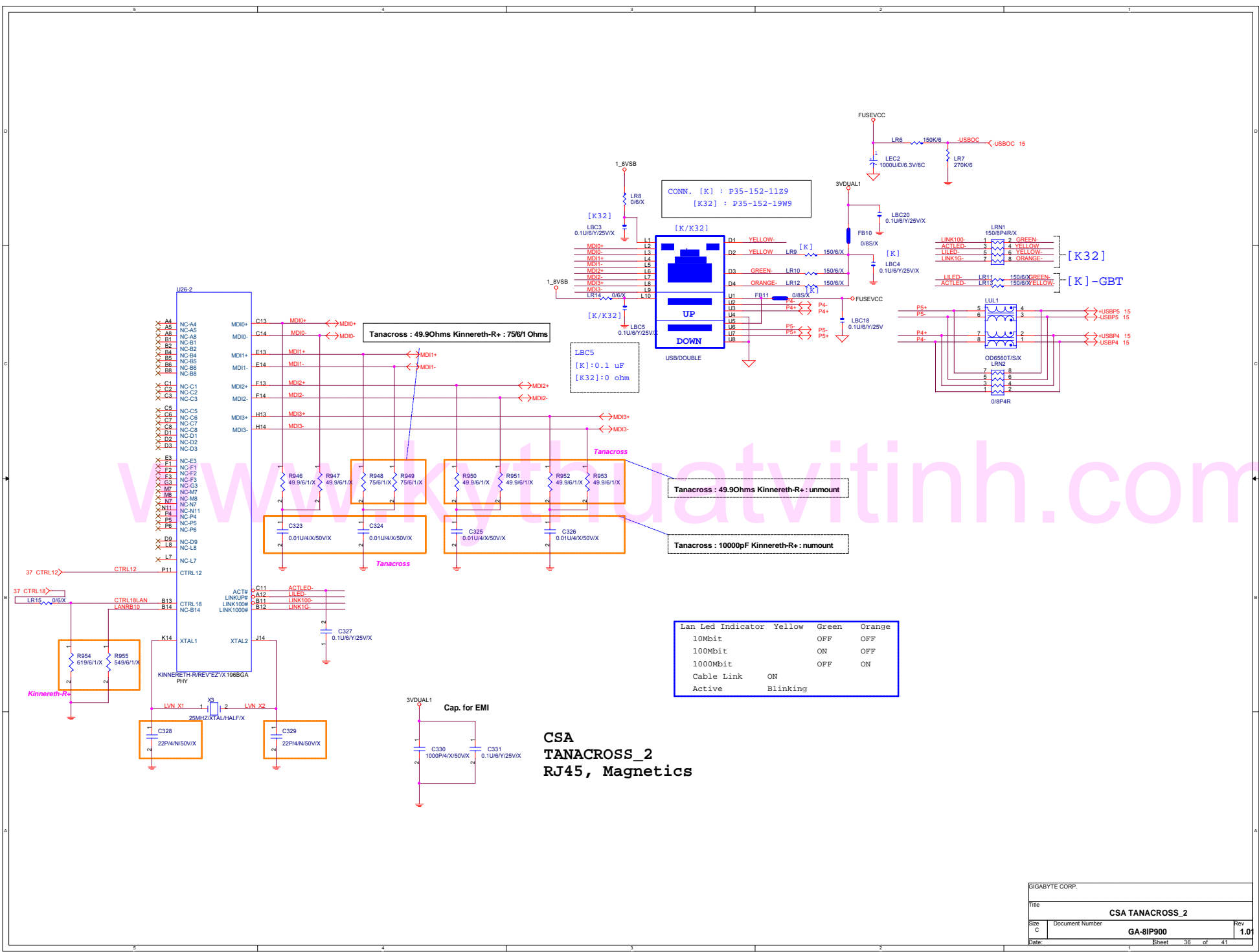


Big Copper to GND

GIGABYTE CORP.		
Title		
Misc. PWR & ATX CONN.		
Size B	Document Number	Rev
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SIGABYTE CORP.			
Title			
<b>CSA TANACROSS_1</b>			
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Tanacross : 49.90hms Kinnereth-R+ : 756/1 Ohms

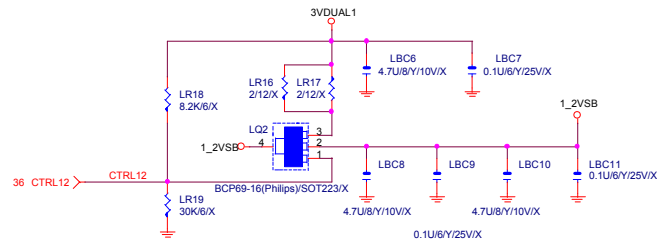
Tanacross : 49.90hms Kinnereth-R+ : numount

Tanacross : 10000pF Kinnereth-R+ : numount

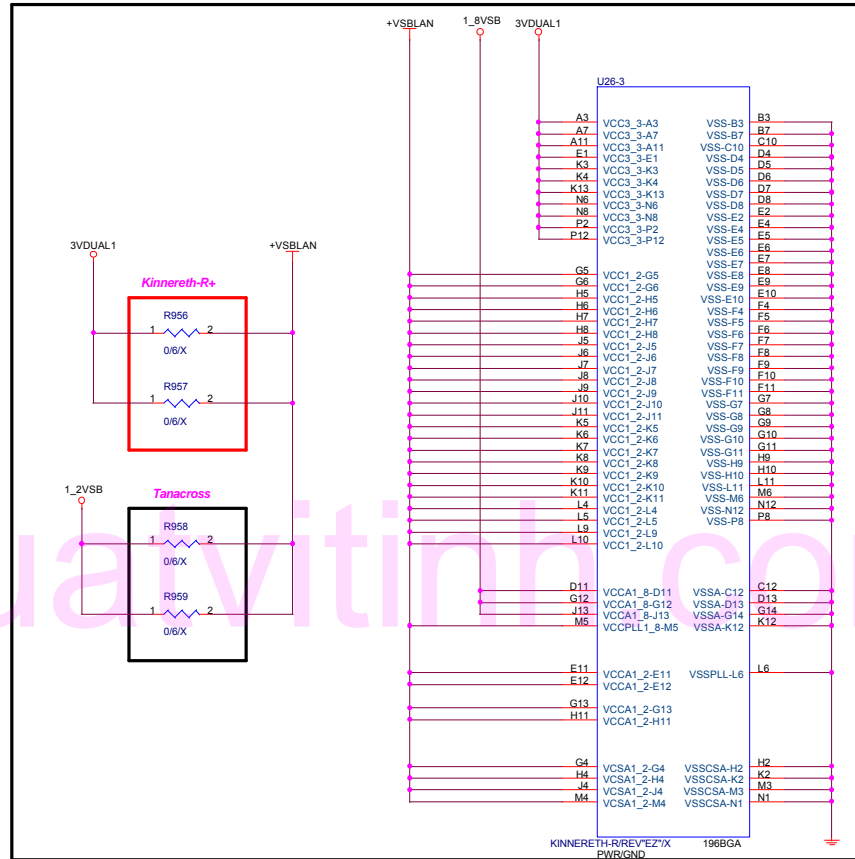
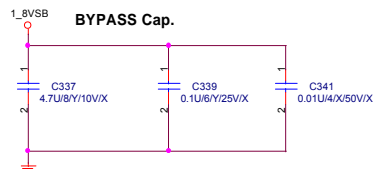
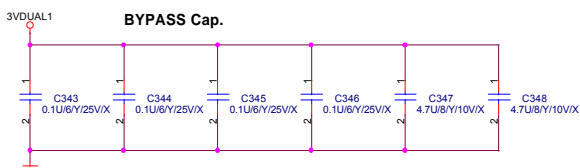
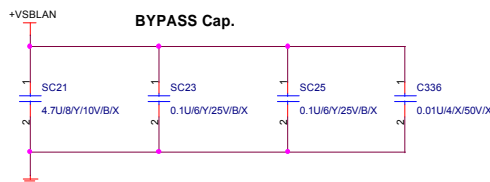
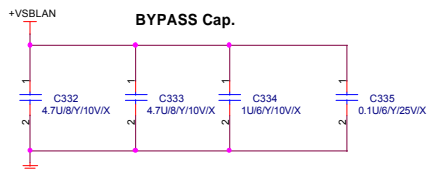
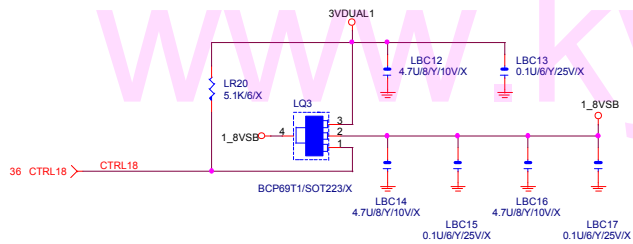
Lan Led Indicator	Yellow	Green	Orange
10Mbit		OFF	OFF
100Mbit		ON	OFF
1000Mbit		OFF	ON
Cable Link	ON		
Active		Blinking	

**CSA  
TANACROSS\_2  
RJ45, Magnetics**

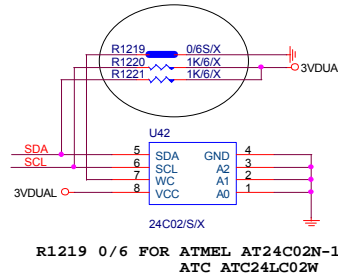
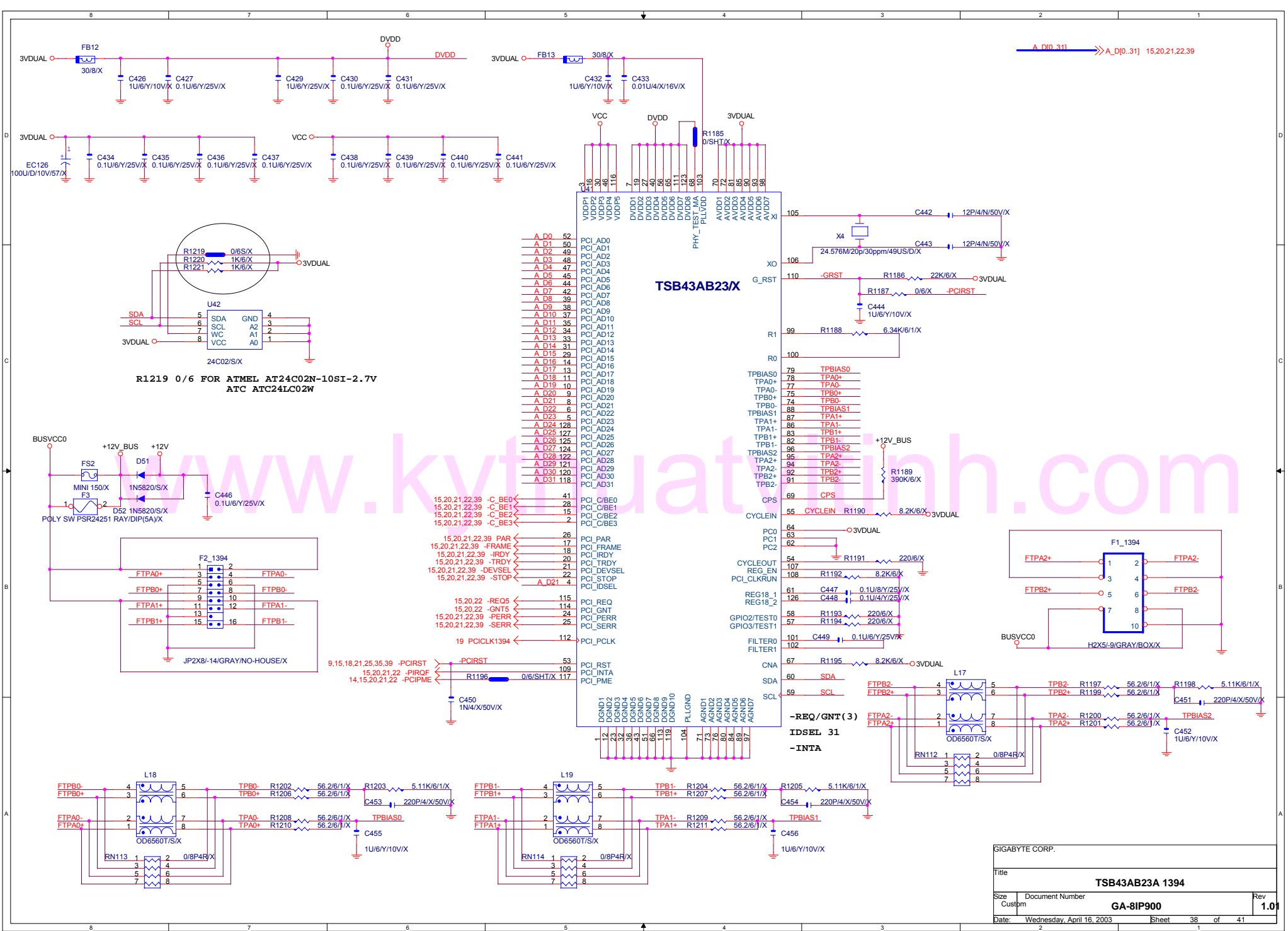
**+1.2VSB**  
Max800mA Typ500mA



**+1.8VSB**  
Max500mA Typ250mA



SISGABYTE CORP.			
Title			
<b>CSA TANACROSS_3</b>			
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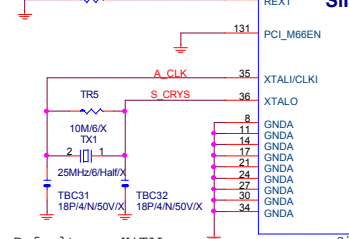
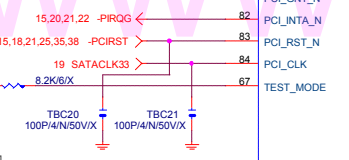
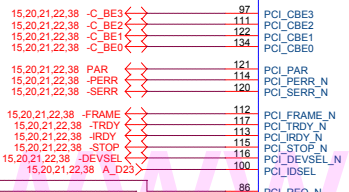
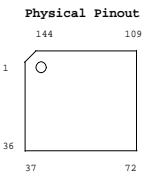
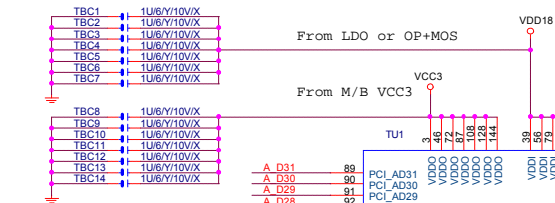


A_D0	52	PCI_AD0
A_D1	50	PCI_AD1
A_D2	49	PCI_AD2
A_D3	48	PCI_AD3
A_D4	47	PCI_AD4
A_D5	45	PCI_AD5
A_D6	44	PCI_AD6
A_D7	42	PCI_AD7
A_D8	39	PCI_AD8
A_D9	38	PCI_AD9
A_D10	37	PCI_AD10
A_D11	35	PCI_AD11
A_D12	34	PCI_AD12
A_D13	33	PCI_AD13
A_D14	31	PCI_AD14
A_D15	29	PCI_AD15
A_D16	14	PCI_AD16
A_D17	13	PCI_AD17
A_D18	11	PCI_AD18
A_D19	10	PCI_AD19
A_D20	9	PCI_AD20
A_D21	8	PCI_AD21
A_D22	6	PCI_AD22
A_D23	5	PCI_AD23
A_D24	128	PCI_AD24
A_D25	127	PCI_AD25
A_D26	125	PCI_AD26
A_D27	124	PCI_AD27
A_D28	122	PCI_AD28
A_D29	121	PCI_AD29
A_D30	120	PCI_AD30
A_D31	118	PCI_AD31

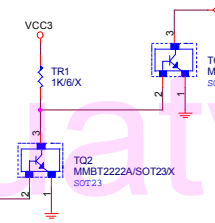
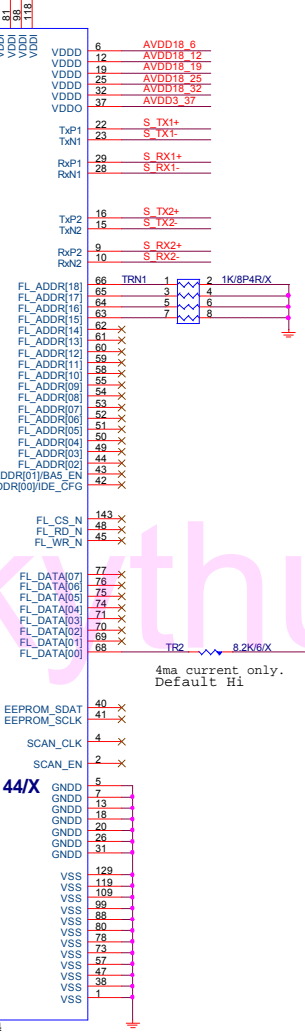
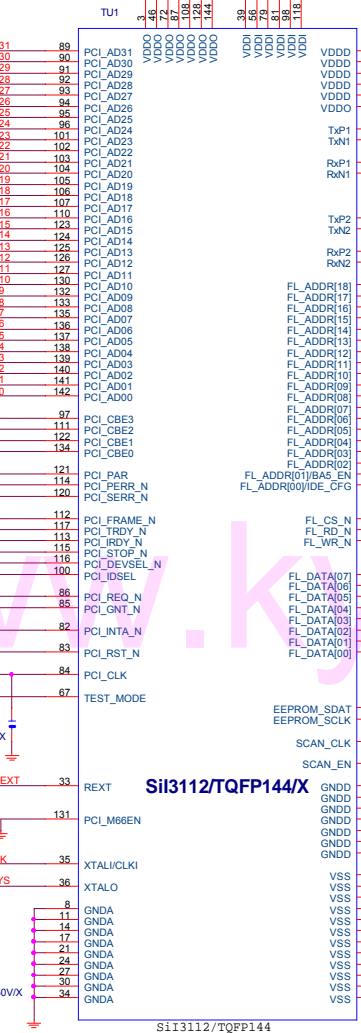
15,20,21,22,39	-C_BE0	11
15,20,21,22,39	-C_BE1	28
15,20,21,22,39	-C_BE2	15
15,20,21,22,39	-C_BE3	2
15,20,21,22,39	PAR	26
15,20,21,22,39	-FRAME	17
15,20,21,22,39	-IRDY	18
15,20,21,22,39	-TRDY	20
15,20,21,22,39	-TRDY	20
15,20,21,22,39	-DEVSEL	21
15,20,21,22,39	-STOP	22
15,20,22	-REQ0	115
15,20,22	-GNT5	114
15,20,21,22,39	-PERR	24
15,20,21,22,39	-SERR	25
19	POCLK1394	112

9,15,18,21,25,35,39	-PCIRST	53
15,20,21,22	-PIRQF	109
14,15,20,21,22	-PCIPME	117

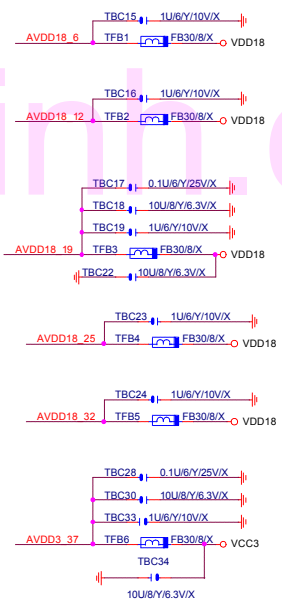
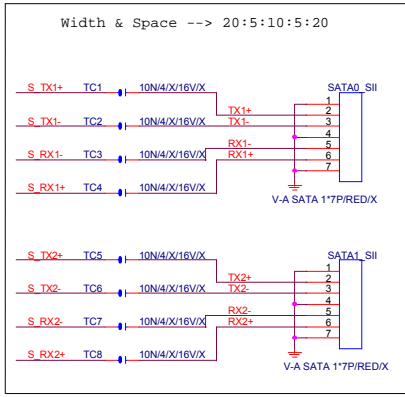
GIGABYTE CORP.		
Title		
TSB43AB23A 1394		
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Default use X'TAL



Place IC VCC3 四邊



L-C close to each Power pin (6, 12, 19, 25, 32, 27)

1. TX+/- & RX+/- 儘可能Reference GND, 換層時須在其Via hole旁5mil處左右各打一個GND Via.
2. TX+/- & RX+/-兩旁最好能包地.



<b>GIGABYTE</b>			
Silicon Image SiI3112(S-ATA)			
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# GIGABYTE GA-8IG1000 Pro PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	REQ01-	GNT01-
PCI SLOT2	17	F,G,A,C	PCLK1	REQ02-	GNT02-
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-
TI 1394	21	F	PCICLK1394	REQ5-(REQB#)	GNT5-(GNTB#)
SATA SI3112A	23	G	SATACLK33	GPO0(REQA#)	GPO16(GNTA#)

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PCI ROUNT LIST			
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# GIGABYTE GA-8IG1000 Pro GPIO LIST

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIP	I/O	FUNCTION
GPO23	NA	PULL 8.2K TO VCC3
GPO24	O	INTEL LAN ENABLE/DISABLE.
GPO25	O	FRONT PANEL -MPD.
GPO27	O	FRONT PANEL +MPD.
GPO28	O	GREEN LED
GPO32	O	BIOS WRITE PROTECT.
GPO33	O	SATA LED.
GPO34	I	CLEAR PASSWORD.